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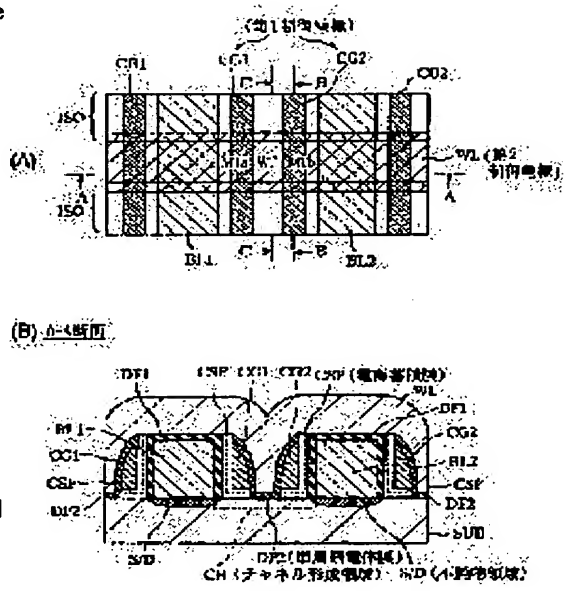
(54) NONVOLATILE SEMICONDUCTOR STORAGE DEVICE AND ITS MANUFACTURING METHOD

(57)Abstract:

PROBLEM TO BE SOLVED: To prevent the occurrence of conductive residues that short-circuit word lines to each other.

SOLUTION: The memory cell of a nonvolatile semiconductor storage device has a channel forming area CH, a charge storing film CSF composed of a plurality of laminated dielectric films, and two storing sections composed the areas of the charge storing films CSF overlapping both end sections of the channel forming area CH. The storage device also has single-layer dielectric films DF2 which come in contact with the surface of the channel forming area CH between the storing sections, auxiliary layers (for example, bit lines BL1 and BL2) respectively formed on two impurity areas S/D, and two first control electrodes CG1 and CG2 which are formed on the auxiliary layers through the dielectric films DF2 and positioned on the storing sections. In addition, the storage device also has second control electrodes WL which are buried in the space between the first control electrodes CG1 and CG2 in a state where the electrodes WL are insulated from the electrodes CG1 and CG2 and brought into contact with the dielectric films DF2. Since the main areas of the facing surfaces of the first control electrodes CG1 and CG2 are forwardly tapered, no conductive residue is left during working the second control electrodes WL.



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CLAIMS

[Claim(s)]
[Claim 1] The channel formation field where it has a memory cell and the memory cell concerned consists of a semi-conductor, The charge storage film with [consist of two or more dielectric films by which the laminating was carried out, and] charge maintenance capacity, The two storage sections which consist of fields of the above-mentioned charge storage film which laps on the both ends of the above-mentioned channel formation field, The dielectric film of the monolayer which touched on the above-mentioned channel formation field between the above-mentioned storage sections, The 1st two control electrode formed at a time on [each / one] the above-mentioned storage section so that the main fields of the field which counters mutually might become forward tapered shape-like, A non-volatile semiconductor memory with the 2nd control electrode which was embedded in the condition of having insulated with each 1st control electrode, to the tooth space between the 1st two above-mentioned control electrode, and touched on the dielectric film of the above-mentioned monolayer.
[Claim 2] A non-volatile semiconductor memory according to claim 1 further with two auxiliary layers close to each field where the above-mentioned memory cell consisted of a semi-conductor of the above-mentioned channel formation field and a reverse conductivity type, was respectively formed on two impurity ranges mutually estranged across a channel formation field, and the two above-mentioned impurity ranges, and faced the outside of the above-mentioned memory cell of the 1st control electrode of the above.
[Claim 3] The above-mentioned auxiliary layer is a non-volatile semiconductor memory according to claim 2 which consists of a conductive layer which approached the lateral surface of the 1st control electrode of the above in the condition of having made the dielectric film intervening.
[Claim 4] The above-mentioned conductive layer is a non-volatile semiconductor memory according to claim 3 which consists of a layer of the polycrystal silicon with which the impurity of the same conductivity type as the above-mentioned impurity range was introduced, or amorphous silicon.
[Claim 5] The above-mentioned auxiliary layer is a non-volatile semiconductor memory according to claim 2 which consists of a dielectric layer close to the lateral surface of the 1st control electrode of the above.
[Claim 6] The above-mentioned channel formation field, the two above-mentioned storage sections, the 1st and 2nd control electrodes of the above, Two or more arrangement of the two above-mentioned auxiliary layers and the memory cell with the two above-mentioned impurity ranges is carried out at the letter of a matrix, and a memory cell array is constituted. The two above-mentioned auxiliary layers are arranged for a long time in the direction of a train, respectively, and it is shared between two or more memory cells. It is shared between two memory cells which adjoined the line writing direction. And the 1st two above-mentioned control electrode The non-volatile semiconductor memory according to claim 2 which it has been arranged along with the two above-mentioned auxiliary layers, and it was shared between two or more memory cells, and the 2nd control electrode of the above has been arranged for a long time at the line writing direction, and was shared between two or more memory cells.
[Claim 7] The non-volatile semiconductor memory according to claim 6 through which the 1st two

control electrode of the above whose above-mentioned auxiliary layer shared between two memory cells which adjoined the line writing direction is pinched from crosswise both sides has flowed electrically.
[Claim 8] The non-volatile semiconductor memory according to claim 7 to which the 1st control electrode of the above became from the conductive layer of the sidewall configuration formed in the crosswise both sides of the above-mentioned auxiliary layer, and the 1st two control electrode of each other with the above-mentioned sidewall configuration was connected on the outside of the above-mentioned memory cell array.
[Claim 9] The 1st control electrode of the above is a non-volatile semiconductor memory according to claim 7 which consists two side faces and top faces of the above-mentioned auxiliary layer of a wrap conductive layer.
[Claim 10] The non-volatile semiconductor memory according to claim 6 with which the dielectric detached core which separates the above-mentioned channel formation field electrically between the memory cells which adjoined in the direction of a train was formed in the surface field of the above-mentioned semi-conductor between the 2nd control electrode of the above at least.
[Claim 11] The 2nd control electrode of the above is the non-volatile semiconductor memory according to claim 10 with which it has a sidewall on the crosswise both sides, and each of the sidewall concerned lapped on the edge of the above-mentioned dielectric detached core.
[Claim 12] The channel formation field where it has two or more memory cells, and each memory cell consists of the 1st conductivity-type semi-conductor, The 1st and 2nd impurity ranges which consisted of the 2nd conductivity-type semi-conductor, and were mutually estranged across the above-mentioned channel formation field, alienation of the 1st and 2nd impurity ranges of the above -- with the control electrode which has been arranged for a long time in a direction and the direction which intersects perpendicularly, and was shared between two or more memory cells Consist of two or more dielectric films formed in the layer immediately under the above-mentioned control electrode, and it has the charge storage film which memorizes information into the part which lapped on the above-mentioned channel formation field. The memory cell which adjoins in a direction and the direction which intersects perpendicularly is electrically separated by the dielectric detached core. alienation of the 1st and 2nd impurity ranges of the above -- The non-volatile semiconductor memory to which the 1st above-mentioned impurity range and the 2nd above-mentioned impurity range of the above-mentioned contiguity memory cell which were separated by the above-mentioned dielectric detached core were connected by the conductive layer, respectively.
[Claim 13] The channel formation field which consists of the 1st conductivity-type semi-conductor, and two impurity ranges which estrange across the above-mentioned channel formation field, and consist of the 2nd conductivity-type semi-conductors, The 1st two control electrode formed in the condition of having made the charge storage film which consists of two or more dielectric films intervening on the both ends of the above-mentioned channel formation field near the two above-mentioned impurity ranges, It meets in the condition of having made the dielectric film of a monolayer intervening on the above-mentioned channel formation field between the 1st control electrode. It is the manufacture approach of a non-volatile semiconductor memory with the 2nd control electrode arranged for a long time in the direction. alienation of the above-mentioned impurity range -- An auxiliary layer with the Rhine configuration long in a direction and the direction which intersects perpendicularly is formed on the semiconductor region in which the above-mentioned impurity range top or the above-mentioned impurity range is formed. many processes of the following [approach / above-mentioned / manufacture], i.e., alienation of the above-mentioned impurity range, -- The above-mentioned charge storage film is formed on the front face of the above-mentioned auxiliary layer, and the front face of the above-mentioned channel formation field. Along with the above-mentioned auxiliary layer, the 1st control electrode of the above is formed in the condition of having made the above-mentioned charge storage film intervening. Etching which used the 1st control electrode of the above as the mask removes some charge storage film. The manufacture approach of a non-volatile semiconductor memory including

each process which forms the dielectric film of a monolayer in the front face of the above-mentioned channel formation field and the front face of the 1st control electrode of the above which were exposed by removal of the above-mentioned charge storage film, and forms the 2nd control electrode of the above on the dielectric film of the above-mentioned monolayer, and the above-mentioned auxiliary layer.
[Claim 14] The above-mentioned auxiliary layer is the manufacture approach of the non-volatile semiconductor memory according to claim 13 which consists of a dielectric layer.
[Claim 15] The above-mentioned auxiliary layer is the manufacture approach of the non-volatile semiconductor memory according to claim 13 which consists of a conductive layer.
[Claim 16] The above-mentioned auxiliary layer is the manufacture approach of the non-volatile semiconductor memory according to claim 15 which consists of the polycrystal silicon or amorphous silicon with which the 2nd conductivity-type impurity was introduced.
[Claim 17] The manufacture approach of the non-volatile semiconductor memory according to claim 16 which includes further the process which forms the impurity range of the 2nd conductivity type of the above by solid phase diffusion which made the above-mentioned auxiliary layer the source of diffusion.
[Claim 18] The manufacture approach of the non-volatile semiconductor memory according to claim 16 which includes further the process which oxidizes thermally alternatively the front face of the polycrystal silicon which makes the above-mentioned auxiliary layer, or amorphous silicon in order to insulate between the 2nd control electrode of the above, and the above-mentioned auxiliary layers.
[Claim 19] The formation process of the above-mentioned auxiliary layer carries out the laminating of the following many processes, i.e., pad oxide film, nitrides, and sacrifice layers in this order, and forms a cascade screen. Embed into the part from which etching removed a part of above-mentioned cascade screen, and the above-mentioned cascade screen removed the polycrystal silicon or amorphous silicon with which the 2nd conductivity-type impurity was introduced, and the above-mentioned auxiliary layer is formed. The manufacture approach of a non-volatile semiconductor memory including each process which removes the above-mentioned sacrifice layer and oxidizes thermally the front face of the above-mentioned polycrystal silicon or amorphous silicon by using the above-mentioned nitride as the oxidation inhibition film according to claim 18.
[Claim 20] The manufacture approach of the non-volatile semiconductor memory according to claim 19 which forms the above-mentioned impurity range of the 2nd conductivity type by solid phase diffusion which made the above-mentioned polycrystal silicon or amorphous silicon the source of diffusion in case the front face of the above-mentioned polycrystal silicon or amorphous silicon is oxidized thermally.
[Claim 21] The manufacture approach of the non-volatile semiconductor memory according to claim 19 which includes further each process which embeds the polycrystal silicon or the amorphous silicon with which the formation process of the above-mentioned auxiliary layer formed opening in the above-mentioned cascade screen according to many following processes, i.e., the pattern of the above-mentioned auxiliary layer, the 2nd conductivity-type impurity was introduced through the above-mentioned opening, the above-mentioned impurity range of the 2nd conductivity type was formed in the semiconductor region exposed to the above-mentioned opening base, and the impurity was introduced at the above-mentioned opening circles.
[Claim 22] The manufacture approach of the non-volatile semiconductor memory according to claim 13 which forms the 1st control electrode of a sidewall configuration in the crosswise both sides of the above-mentioned auxiliary layer by depositing and carrying out etchback of the electric conduction film in the formation process of the 1st control electrode of the above.
[Claim 23] The manufacture approach of a non-volatile semiconductor memory according to claim 13 of containing further each process dissociate the above-mentioned electric-conduction film in the part which etches the above-mentioned electric-conduction film while the formation process of the 1st control electrode of the above deposits the electric-conduction film, forms an etching protective layer on the electric-conduction film located above the above-mentioned auxiliary layer and protects the upper part part of an auxiliary layer by the etching protective layer, and is located above the center

section of the above-mentioned channel formation field.
[Claim 24] The manufacture approach of a non-volatile semiconductor memory according to claim 23 of containing further each process the formation process of the above-mentioned etching protective layer forms the oxidation inhibition film in the wall of the crevice of the above-mentioned electric-conduction film made reflecting the configuration of the above-mentioned auxiliary layer, and oxidize thermally the front face of the electric-conduction film part are located above the above-mentioned auxiliary layer which is not covered with the oxidation inhibition film, form the above-mentioned etching protective layer, and remove the above-mentioned oxidation inhibition film.
[Claim 25] The manufacture approach of the non-volatile semiconductor memory according to claim 13 which includes further each process which forms the dielectric detached core of the shape of long parallel Rhine in an one direction at the semi-conductor of the 1st conductivity type, forms the auxiliary layer which consists of the polycrystal silicon or the amorphous silicon with which the impurity was introduced in the shape of [long] parallel Rhine in the direction which intersects perpendicularly with the above-mentioned dielectric detached core, and forms the above-mentioned impurity range of the 2nd conductivity type in the semi-conductor part which laps with the arrangement field of the above-mentioned auxiliary layer between the above-mentioned dielectric detached cores.
[Claim 26] The manufacture approach of a non-volatile semiconductor memory including each process to which the process which forms the 1st control electrode of the above deposits many following processes, i.e., the electric conduction film with which it becomes the 1st control electrode of the above, forms an etching protective layer on the electric conduction film part used as the drawer field of the 1st control electrode of the above, and carries out etchback of the above-mentioned electric conduction film according to claim 13.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention has the two storage sections which consist of charge storage film to which the both ends of a channel formation field were made to carry out the laminating of two or more dielectric films, and relates 2-bit information to an independently memorizable non-volatile semiconductor memory and its manufacture approach to the storage section concerned.
[0002]
[Description of the Prior Art] Conventionally, it has the charge storage film to which the laminating of two or more dielectric films, such as the so-called MONOS (Metal-Oxide-Nitride-Oxide-Semiconductor) mold, was carried out, and the non-volatile semi-conductor storage element which memorizes information by controlling the amount of charges accumulated in the charge trap in this charge storage

film is known.
[0003] The technique in which 2 bits per one memory cell were independently memorizable was reported by by recently writing binary information in a source [of the charge storage film], and drain side independently with the conventional CHE (Channel Hot Electron) impregnation method paying attention to the ability pouring a charge into a part of distribution field of a discrete charge trap.
[0004] For example, the charge storage film was separated and prepared in the source and drain side, and the control electrode was prepared on the charge storage film, and the WORD gate electrode is prepared in the channel center section between control electrodes "2000 Symposium on VLSI Technology and pp.122-123" in the condition of having made the dielectric film of the monolayer which does not have charge maintenance capacity intervening. A WORD gate electrode is connected to a word line, a control electrode is wired in the direction which intersects perpendicularly with a word line, and a WORD gate electrode is controlled independently. For this reason, the controllability and charge injection efficiency of a location of charge impregnation could be gathered, consequently high-speed writing is attained.
[0005] This memory cell is called a twin MONOS cel, has the WORD gate electrode repeated at fixed spacing to the line writing direction, and has the conductive layer of a sidewall form on the wall surface of those line writing direction both sides. It is ONO (Oxide-Nitride-Oxide) directly under the conductive layer of this sidewall form. It has the film, i.e., the charge storage film with charge maintenance capacity. On the other hand, the dielectric film of a monolayer is formed directly under a WORD gate electrode, therefore this part does not have charge maintenance capacity. N+ which introduces an N type impurity into the substrate part which uses the conductive layer and WORD gate electrode of a sidewall form as a mask, and expresses them between the conductive layers of the adjoining sidewall form, and becomes the source or a drain The impurity range is formed.
[0006]
[Problem(s) to be Solved by the Invention] Although the concrete manufacture approach is not indicated by the above mentioned paper, this twin MONOS cel has a trouble on the manufacture shown below and structure.
[0007] In this twin MONOS cel, after forming a WORD gate electrode, the conductive layer of a sidewall form is formed in that side face. Therefore, the process which connects a WORD gate electrode with a word line is required after that.
[0008] Moreover, it is necessary to carry out pattern NINGU of the WORD gate electrode in this twin MONOS cel at the shape of parallel Rhine long in the direction of a train at first. After usually depositing a WORD gate electrode material at this time, the pattern of a resist is formed on it and an anisotropy processes a WORD gate electrode material by the powerful etching approach (ReactiveIon Etching), for example, RIE, by using this resist as a mask. As for the cross-section configuration of a resist pattern, it is common that a side face serves as a forward tapered shape, and in order that the resist at the time of etching may retreat somewhat, the side face of the WORD gate electrode after processing also serves as a forward tapered shape. Moreover, even if it uses the ingredient which does not retreat at the time of etching without using a resist, a forward tapered shape tends to be somewhat made on the side face of the WORD gate electrode after processing under the effect of the side-attachment-wall affix at the time of etching etc. In case this WORD gate electrode carries out pattern NINGU of after that, for example, the word line, it is necessary to process it into coincidence and to separate it between cels. However, etching must remove a WORD gate electrode alternatively, digging a hole with the cross-section configuration of trapezoidal shape, since the control electrode is formed in the condition of having made the insulator layer already intervening to the side attachment wall of a WORD gate electrode at this time. Therefore, the lower part side of the side face of a back taper-like control electrode is hard to be etched at the time of this etching, and it is easy to produce conductive residue into this part along with a control electrode. If conductive residue arises, it will become short [between word lines / poor].

[0009] Moreover, the conductive layer of a sidewall form goes around the perimeter of the conductive layer of the shape of Rhine used as a WORD gate electrode, and is formed annularly. If the conductive layer of a sidewall form is used as a control electrode as it is, the control electrode by the side of the source and the control electrode by the side of a drain will be in the condition of having connected too hastily electrically. Therefore, in order to impress an electrical potential difference which is different in the control electrode by the side of the source, and the control electrode by the side of a drain, both control electrodes must be separated. Since this separation cannot be performed by bundling up at the time of other processes, for example, word line processing, for example, after only the both-ends side of the conductive layer of the shape of Rhine used as a WORD gate electrode forms the etching mask which carried out opening and removes a wrap insulator layer for the conductive layer of a sidewall form through this opening, the process which disconnects a conductive layer by etching is needed.
[0010] Furthermore, in the twin MONOS cel, since the ONO film is formed directly under the conductive layer of a sidewall form, the ONO film which touches a channel formation field has been prolonged for a long time in the direction of a train along with the conductive layer of a sidewall form. Elimination is performed by pouring a charge into the ONO film field (henceforth the storage section) which intersects a channel, and writing being performed, and drawing out stored charge to a substrate side, or pouring in the charge of a reverse conductivity type to this storage section, at the time of actuation. The adjoining field of the storage section becomes easy to be covered with a charge while repeating this rewriting actuation repeatedly regularly. And leak pass becomes easy to be made into the outside of a channel with this charge. When drawing out and eliminating the accumulated charge from the whole channel surface by the electron, like the storage section, the adjoining field is also under rule of a control electrode, and since the electron collected on the adjoining field also draws out and withers in coincidence, it seldom becomes a problem. However, since it will become easy to produce leak pass if the adjoining field of the storage section is covered with the electron hole of the case of a charge with the polarity of the direction which turns on a channel, for example, an N type channel, when pouring the charge of reversed polarity into the storage section, in order to eliminate the charge accumulated especially, the fall of the leak property by this poses a problem.
[0011] The 1st purpose of this invention is by making possible the structure top of forming a WORD gate electrode as a word line (the 2nd control electrode) and one to make unnecessary the process which connects a word line with a WORD gate electrode. The 2nd purpose of this invention is to make into structure top needlessness the process for preventing generating of conductive residue which short-circuits between word lines, and cutting between two control electrodes in the same cel. The 3rd purpose of this invention is to make for an unnecessary charge to collect between the adjoining field of the direction which met the control electrode to the storage section, or the storage section into the structure which is prevented and leakage current does not generate.
[0012]
[Means for Solving the Problem] In order to attain the 1st and 2nd purposes of the above, the non-volatile semiconductor memory concerning the 1st viewpoint of this invention The channel formation field where it has a memory cell and the memory cell concerned consists of a semi-conductor, The charge storage film with [consist of two or more dielectric films by which the laminating was carried out, and] charge maintenance capacity, The two storage sections which consist of fields of the above-mentioned charge storage film which laps on the both ends of the above-mentioned channel formation field, The dielectric film of the monolayer which touched on the above-mentioned channel formation field between the above-mentioned storage sections, The 1st two control electrode formed at a time on [each / one] the above-mentioned storage section so that the main fields of the field which counters mutually might become forward tapered shape-like, It has the 2nd control electrode which was embedded in the condition of having insulated with each 1st control electrode, to the tooth space between the 1st two above-mentioned control electrode, and touched on the dielectric film of the above-mentioned monolayer. Moreover, the above-mentioned memory cell consists of a semi-conductor

of the above-mentioned channel formation field and a reverse conductivity type, and it is respectively formed on two impurity ranges mutually estranged across a channel formation field, and the two above-mentioned impurity ranges, and has further two auxiliary layers close to each field facing the outside of the above-mentioned memory cell of the 1st control electrode of the above.

[0013] The above-mentioned auxiliary layer approaches the 1st control electrode of the above in the condition of having made the dielectric film intervening, suitably, and consists of a layer of the polycrystal silicon with which the impurity of the same conductivity type as a conductive layer or the above-mentioned impurity range was introduced, or amorphous silicon. Or the above-mentioned auxiliary layer consists of a dielectric layer close to the 1st control electrode of the above.

[0014] In the configuration which has arranged two or more memory cells in the shape of a matrix, its potato is good, using as the configuration good [as a sidewall form] and connected [the configuration] mutually in the upper part of an auxiliary layer the 1st two control electrode of the above whose above-mentioned auxiliary layer shared between two memory cells which adjoined the line writing direction is pinched from crosswise both sides. The 1st control electrode of the latter configuration consists two side faces and top faces of the above-mentioned auxiliary layer of a wrap conductive layer, and its wiring resistance is low compared with a sidewall form.

[0015] In order to attain the 3rd purpose of the above, the non-volatile semiconductor memory concerning the 2nd viewpoint of this invention The channel formation field where it has two or more memory cells, and each memory cell consists of the 1st conductivity-type semi-conductor, The 1st and 2nd impurity ranges which consisted of the 2nd conductivity-type semi-conductor, and were mutually estranged across the above-mentioned channel formation field, alienation of the 1st and 2nd impurity ranges of the above -- with the control electrode which has been arranged for a long time in a direction and the direction which intersects perpendicularly, and was shared between two or more memory cells Consist of two or more dielectric films formed in the layer immediately under the above-mentioned control electrode, and it has the charge storage film which memorizes information into the part which lapped on the above-mentioned channel formation field. The memory cell which adjoins in a direction and the direction which intersects perpendicularly is electrically separated by the dielectric detached core. alienation of the 1st and 2nd impurity ranges of the above -- The 1st above-mentioned impurity range and the 2nd above-mentioned impurity range of the above-mentioned contiguity memory cell which were separated by the above-mentioned dielectric detached core are connected by the conductive layer, respectively.

[0016] In order to attain the 1st and 2nd purposes of the above, the manufacture approach of the non-volatile semiconductor memory concerning the 3rd viewpoint of this invention The channel formation field which consists of the 1st conductivity-type semi-conductor, and two impurity ranges which estrange across the above-mentioned channel formation field, and consist of the 2nd conductivity-type semi-conductors, The 1st two control electrode formed in the condition of having made the charge storage film which consists of two or more dielectric films intervening on the both ends of the above-mentioned channel formation field near the two above-mentioned impurity ranges, It meets in the condition of having made the dielectric film of a monolayer intervening on the above-mentioned channel formation field between the 1st control electrode of the above. It is the manufacture approach of a non-volatile semiconductor memory with the 2nd control electrode arranged for a long time in the direction. alienation of the above-mentioned impurity range -- An auxiliary layer with the Rhine configuration long in a direction and the direction which intersects perpendicularly is formed on the semiconductor region in which the above-mentioned impurity range top or the above-mentioned impurity range is formed. many processes of the following [approach / above-mentioned / manufacture], i.e., alienation of the above-mentioned impurity range, -- The above-mentioned charge storage film is formed on the front face of the above-mentioned auxiliary layer, and the front face of the above-mentioned channel formation field. Along with the above-mentioned auxiliary layer, the 1st control electrode of the above is formed in the condition of having made the above-mentioned charge storage film intervening. Etching

which used the 1st control electrode of the above as the mask removes some charge storage film. Each process which forms the dielectric film of a monolayer in the front face of the above-mentioned channel formation field and the front face of the 1st control electrode of the above which were exposed by removal of the above-mentioned charge storage film, and forms the 2nd control electrode of the above in the dielectric film and the above-mentioned auxiliary layer of the above-mentioned monolayer is included.

[0017] In the manufacture approach of the non-volatile semiconductor memory applied to the 3rd above mentioned viewpoint in order to attain the 3rd purpose of the above The dielectric detached core of the shape of long parallel Rhine is formed in an one direction at the semi-conductor of the 1st conductivity type. Each process which forms the auxiliary layer which consists of the polycrystal silicon or amorphous silicon with which the impurity was introduced in the shape of [long] parallel Rhine in the direction which intersects perpendicularly with the above-mentioned dielectric detached core, and forms the above-mentioned impurity range of the 2nd conductivity type in the semi-conductor part which laps with the arrangement field of the above-mentioned auxiliary layer between the above-mentioned dielectric detached cores is included further.

[0018] Since the fields where the opposed face of the 1st two control electrode which constitutes one memory cell is main become forward tapered shape-like according to the manufacture approach of the non-volatile semiconductor memory concerning the 1st viewpoint of this invention, and the non-volatile semiconductor memory concerning the 3rd viewpoint, in case the 2nd control electrode is processed, the residue of conductive material which short-circuits between the 2nd control electrode does not occur. Moreover, formation of a word line is completed only by processing the 2nd control electrode. According to the non-volatile semiconductor memory concerning the 2nd viewpoint of this invention, the field of the charge storage film which adjoined the longitudinal direction both sides of the 1st control electrode to the charge storage film part used as the storage section has run aground on the dielectric detached core between channel formation fields. only by setting thickness of a dielectric detached core to about dozens of nm, even when a charge is accumulated in this adjoining field, from before, the effect to the semi-conductor directly under a dielectric detached core of that charge is markedly alike, and can weaken.

[0019]

[Embodiment of the Invention] Hereafter, a memory cell array method makes an example nonvolatile memory of VG (Vertual Ground) mold for the gestalt of operation of this invention using the memory cell of an N type channel, and it explains, referring to a drawing. Drawing 1 (A) is the top view of a memory cell, and drawing 1 (B) is the sectional view which met the A-A line of drawing 1 (A). Moreover, the sectional view where drawing 2 (A) met the B-B line of drawing 1 (A), and drawing 2 (B) are the sectional views which met the C-C line of drawing 1 (A).

[0020] Setting to these drawings, Sign SUB shows various kinds of semi-conductor layers of P type, such as a well or a SOI (Silicon On Insulator) layer of the semi-conductor substrate of P type, and P type. For convenience, it is hereafter called Substrate SUB. On Substrate SUB, the dielectric detached core ISO of the shape of a long parallel stripe is formed in the longitudinal direction (line writing direction) of drawing. the dielectric detached core ISO -- LOCOS (Local Oxidation of Silicon) -- law and STI (Shallow Trench Isolation) -- law or field isolation (Field Isolation) It is formed of any of law they are. Here, the field isolation method is adopted and the dielectric film (dielectric detached core ISO) of the thickness which is about several 10nm is formed on Substrate SUB. The field of the shape of Rhine long to the line writing direction between this dielectric detached core ISO is a semi-conductor active region of the memory cell concerned.

[0021] In the semi-conductor active region, predetermined spacing is set and source drain field S/D into which the N type impurity was introduced is formed. The semi-conductor active region between source drain field S/D is the channel formation field CH of a transistor. The bit lines BL1 and BL2 with which an N type impurity consists of polycrystal silicon introduced into high concentration are formed in the

lengthwise direction (the direction of a train) of drawing which intersects perpendicularly with a line writing direction by the pattern of the shape of long parallel Rhine. Crossing the dielectric detached core ISO top, bit lines BL1 and BL2 contact on source drain field S/D of the memory cell of the direction of a train, and supply a source electrical potential difference common to these memory cells, or a drain electrical potential difference. The thickness of the polycrystal silicon which constitutes bit lines BL1 and BL2 is 100nm - about 500nm. The front face of this polycrystal silicon is covered with the dielectric film DF 1.

[0022] The charge storage film CSF which consists of two or more dielectric films is formed in the condition of having touched on the dielectric film DF 1 of the side face of these bit lines BL1 and BL2, and the edge of a channel formation field. The charge storage film CSF has cross-section the configuration of L characters, and the 1st control electrode (henceforth the control gate) CG1 and CG2 of a sidewall configuration is formed on the pars basilaris ossis occipitalis. The control gates CG1 and CG2 are arranged for a long time in the direction of a train along with bit lines BL1 and BL2 with the charge storage film CSF. Although mentioned later for details, for example the control gates CG1 and CG2 deposit the film of polycrystal silicon, where the front face of bit lines BL1 and BL2 is covered by the dielectric film DF 1 and the charge storage film CSF, and are formed by carrying out etchback of this. The control gates CG1 and CG2 are supported in the condition of having made the dielectric film placed between the side faces of bit lines BL1 and BL2. Therefore, bit lines BL1 and BL2 function as an "auxiliary layer" to the control gates CG1 and CG2. Moreover, the pars basilaris ossis occipitalis of the charge storage film part CSF pinched by control electrodes CG1 and CG2 and the channel formation field CH, i.e., the charge storage film, turns into the "storage section" in which impregnation are recording of the charge is carried out, and informational storage is performed.

[0023] The fields where the opposed face between the control gates CG [CG1 and] 2 is main serve as a forward tapered shape. The advantage of this opposed face serving as a forward tapered shape is mentioned later. The dielectric film DF 2 of a monolayer is formed on the opposed face of the control gates CG1 and CG2, and the channel formation field CH. The word line WL is formed with the conductive material which fills the space between this control gate. The word line WL is formed by the almost same pattern as a semi-conductor active region, crossing the dielectric film DF 1 top on bit lines BL [BL1 and] 2. Moreover, sidewall WL' which consists of conductive material is formed in the side face of the crosswise both sides of a word line WL.

[0024] The reason for having prepared sidewall WL' is as follows. In order to make cell size of the direction of a train into min, it is desirable to form Rhine of the dielectric detached core ISO, Rhine of a tooth space and a word line WL, and a tooth space with the minimum line width F decided [both] by the resolution limit of a photolithography etc. It becomes impossible in that case, for the width of face of the semi-conductor active region which is the tooth-space width of face of the dielectric detached core ISO to take both makeshift allowances almost in accordance with the width of face of a word line WL inevitably. Therefore, in the opposite tooth space between the control gates CG [CG1 and] 2 shown in drawing 2 (B), if a word line WL shifts crosswise to a semi-conductor active region (channel formation field CH), the field which does not lap with a word line WL in a part of channel formation field CH will be made. In order that this field may not receive rule of the electric field by the word line WL, it serves as the source and leak pass between drains, consequently it becomes impossible to make a channel an OFF state. When a word line shifts crosswise especially, the field where a hot electron is not poured into storage **** is made. However, when eliminating using hot hole impregnation, since this storage **** is under electric-field rule of the control gate, a hot hole will be poured in, only the threshold electrical potential difference of the semi-conductor part [directly under] of it will fall greatly, and leakage current will increase through there. Moreover, there is a problem that channel width decreases by location gap of a word line WL. Reduction of WORD line breadth leads to the fall of a read-out current, and is accompanied by disadvantageous profit of accelerating the fall of the S/N ratio of a read-out signal conjointly with increase of leakage current. With this operation gestalt, it becomes possible to

prevent formation of the leak pass described above though the word line WL was formed with minimum line width F, and reduction of channel width by preparing sidewall WL' which extends the width of face of a word line WL substantially in the side face of a word line WL. In addition, in order to attain this purpose, it is more nearly required than it in whether the width of face of sidewall WL' is the same as the doubling allowances of a photolithography. Moreover, in order to attain this purpose, it becomes important that even the dielectric film DF 2 of that substrate does not etch succeeding the time of processing a word line WL. Because, since sidewall WL' will contact the front face of the direct channel formation field CH when a word line WL shifts crosswise in drawing 2 (B) if the dielectric film DF 2 has not covered the front face of the channel formation field CH completely, it is for avoiding such a situation.

[0025] In the memory cell of such a configuration, series connection of the two memory transistors MTa and MTb which are located in both sides on both sides of the central WORD transistor WT and the WORD transistor WT which make a word line WL the gate, and make the gate the control gates CG1 or CG2 is carried out, and they are formed. Namely, at the time of actuation, the WORD transistor WT operates the channel of two memory transistors MTa and MTb as the source and a drain, and the memory transistors MTa and MTb operate either of source drain field S/D, and the channel of the WORD transistor WT as the source and a drain.

[0026] Drawing 3 is a top view of a memory cell array shown including the pad for the electrode drawers of the control gate. This example of illustration corresponds to the control approach which controls control gate CG1 comrades of bit line both sides, control gate CG2 comrades, and control gate CG3 comrades by this potential. With this operation gestalt, since the control gate consists of a conductive layer of the sidewall form formed in the perimeter of a bit line, the two control gates CG1 and CG2 in one memory cell, i.e., the control gates, and the control gates CG2 and CG3 have already been separated at the time of control gate formation. Therefore, it is not necessary to cut the two control gates in one memory cell.

[0027] At the time of control gate formation, in order to form the control pads CP1, CP2, and CP3, after depositing the electric conduction film used as the control gate, the etching protective layer of a rectangle pattern with a big area is formed in the field which forms the control pads CP1, CP2, and CP3, and etchback is performed after that. If an etching protective layer is removed after etchback, the control pads CP1, CP2, and CP3 will be left behind to the part. Drawing 3 is the example which formed the control pad so that it might connect with the shorter side of the annular control gate. In addition, in order to raise the degree of freedom of a serial access between the memory cells of a line writing direction, the process which cuts the control gate of bit line both sides is needed and formation of a control pad is separately needed to the cut control gate to impress a different electrical potential difference independently of the control gate between the adjoining cels.

[0028] Drawing 4 is the sectional view expanding and showing a part for the principal part of a memory cell. As shown in this drawing 4 , the charge storage film CSF consists of dielectric films of three layers. The bottom film BTM of the lowest layer and the top film TOP of the maximum upper layer consist of a silicon dioxide, oxidation silicon nitride (silicon oxynitride), or silicon nitride with few charge traps. The bottom film BTM functions as a potential barrier between substrates, stored charge has extracted the top film TOP enough to the gate side, and it functions as film which prevents that a gate side to a charge enters [an unnecessary charge]. Many charge traps are contained in the middle film CS, and it functions as film which mainly bears a charge storage. The middle film CS is constituted by the insulating matter (dielectric) which consists of the silicon nitride containing many charge traps, oxidation silicon nitride, or a metallic oxide.

[0029] When performing charge impregnation in the storage section 1 at the time of writing, reference voltage is impressed to a bit line BL1 at a forward drain electrical potential difference and a bit line BL2, the forward electrical potential difference optimized by the control gates CG1 and CG2 according to the individual is impressed, and the forward electrical potential difference of extent which forms a channel in a word line WL is impressed. At this time, high energy is obtained by the source drain field S/D side by

which the electron supplied to the channel from source drain field S/D connected to the bit line BL2 had the inside of a channel accelerated, and was connected to the bit line BL1, and it is poured in and accumulated in the storage section 1 over the potential barrier of the bottom film BTM. When pouring a charge into the storage section 2, the electrical potential difference between the control gates CG [CG1 and] 2 is changed, and the electrical potential difference between bit lines BL [BL1 and] 2 is changed. This becomes opposite to the case where the side to which an electron becomes hot in energy an electronic supply side is the above, and an electron is poured into the storage section 2.

[0030] At the time of read-out, a predetermined read-out drain electrical potential difference is impressed among bit lines BL [BL1 and] 2 so that the storage section side in which the bit for read-out was written may serve as the source. Moreover, although a channel may be made to turn on, it is low to extent to which the threshold electrical potential difference of the memory transistors MTa and MTb is not changed, and the forward electrical potential difference optimized, respectively is impressed to the control gates CG1 and CG2 and a word line WL. At this time, the conductivity of a channel changes with the differences between the amount of stored charge of the storage section for read-out, or the existence of a charge effectively, consequently storage information is changed and read to the amount of currents or the potential difference by the side of a drain. When reading another bit, it reads like the above by changing a bit line electrical potential difference, and changing control gate voltage so that the storage section side in which the bit was written may serve as the source.

[0031] At the time of elimination, a channel formation field CH and source drain field S/D side is high, and the blanking voltage of hard flow is impressed to it at the time of the above-mentioned writing so that the control gate electrode 1 CG [CG and] 2 side may become low. Thereby, stored charge is drawn out from one side or the both sides of the storage section at Substrate SUB side, and a memory transistor returns to an elimination condition. In addition, the approach of pouring into the storage section is also employable by generating as other elimination approaches near the PN junction which a source drain field S/D side or the interior of a substrate does not illustrate, and drawing near the high energy charge of reversed polarity by the electric field of the control gate with stored charge.

[0032] It explains referring to the sectional view showing the manufacture approach of a memory cell in drawing 11 from drawing 5 next. First, on Substrate SUB, as shown in drawing 1 (A) and drawing 3 , the dielectric detached core ISO of the shape of an parallel stripe long in the direction of a train is formed. The whole surface on the semi-conductor active region between the dielectric detached cores ISO on the dielectric detached core ISO, as shown in drawing 5 , sequential formation of the pad layer PAD, the oxidation blocking layer OS, and the sacrifice layer SF is carried out. The oxidation blocking layer OS is the precise film which cannot oxidize easily, for example, consists of film of about 50nm silicon nitride. The pad layer PAD under it is thin film formed if needed for the purpose of the improvement in adhesion and stress relaxation to the substrate SUB of the oxidation blocking layer OS, for example, consists of film of a 5nm - about 8nm silicon dioxide. The sacrifice layer SF consists of the film, for example, the silicon dioxide film, of an ingredient with the high selectivity at the time of etching to the oxidization blocking layer OS, and the thickness is decided according to the height of a bit line.

[0033] Pattern NINGU of these cascade screens PAD, OS, and SF is carried out for a resist etc. at a mask, and opening of the shape of a long parallel stripe is formed in the direction of a train. Along with that longitudinal direction, the dielectric detached core ISO and a semi-conductor active region are exposed to these opening circles together with alternation.

[0034] The polycrystal silicon with which the N type impurity was doped by high concentration is deposited thickly, and this is separated from a front face on a sacrifice layer SF front face polish or by carrying out etchback. Thereby, as shown in drawing 7 , the bit lines BL1 and BL2 embedded at opening of cascade screens PAD, OS, and SF are formed. The semi-conductor active region expressing the base of opening circles is electrically connected by bit lines BL1 and BL2.

[0035] After removing the sacrifice layer SF alternatively, the field of the expressed bit lines BL1 and BL2 is oxidized thermally, for example, about several 10nm dielectric film DF 1 is formed. By optimizing

the thickness of a dielectric film DF 1 and the oxidation blocking layer OS, oxidation can fully progress and the end-face side of the oxidation blocking layer OS can also cover completely the front face of bit lines BL1 and BL2 with the dielectric film DF 1 of sufficient thickness. Moreover, at this heating process, an N type impurity is spread in a semi-conductor active region by making into the source of solid phase diffusion the polycrystal silicon which constitutes bit lines BL1 and BL2, consequently source drain field S/D is formed. In addition, it is good to introduce the impurity of required concentration into a semi-conductor active region beforehand only at this diffusion by the ion implantation which an addition is heated, or is the process of previous drawing 6 , and let opening pass when the depth and high impurity concentration of source drain field S/D were inadequate.

[0036] Sequential removal of the oxidization blocking layer OS and the pad layer PAD is carried out, and the charge storage film CSF is formed all over including the expressed channel formation field CH and the front face of a dielectric film DF 1. In addition, when the charge storage film CSF forms the bottom film BTM by thermal oxidation by the three-tiered structure shown in drawing 4 , the bottom film BMT is formed only in a channel formation field CH front face.

[0037] The polycrystal silicon with which the impurity was fully doped is deposited thickly, and after forming in the required part on polycrystal silicon the etching protective layer for forming the control pads CP1 and CP2 illustrated and mentioned above in drawing 3 , and CP3 --, etchback of the polycrystal silicon is carried out. Thereby, the control gates CG1 and CG2 of a sidewall configuration are formed in the condition of having made dielectric films DF1 and CSF intervening, to the both-sides side of bit lines BL1 and BL2. Moreover, the control gates CG1, CG2, and CG3, the control pads CP1 and CP2 connected suitably at --, and CP3 -- are formed in coincidence. Since control gate width is decided, the thickness of the polycrystal silicon with which the impurity at this time was fully doped is controlled strictly. Then, an etching protective layer is removed.

[0038] In order to consider as the structure of drawing 1 (B), the charge storage film CSF is first etched by using the control gates CG1 and CG2 as a mask. Thereby, the charge storage film part on the channel formation field CH between control electrodes CG [CG1 and] 2 and the upper charge storage film part of bit lines BL1 and BL2 are removed. Next, it oxidizes thermally and the silicon dioxide film is formed in a control electrode CG 1, CG2 front face, and the front face of the channel formation field CH exposed among the control gates CG [CG1 and] 2. Thereby, although the dielectric film DF 2 of a monolayer is formed in the front face of polycrystal silicon or single crystal silicon, since other parts are dielectric films, they are hardly oxidized thermally. In addition, since the thermal oxidation thickness of doped polycrystal silicon becomes about twice the thermal oxidation thickness of single crystal silicon, even when the gate oxidation thickness of a central MOS transistor is thin, the insulation during wiring is secured enough. Then, the electrical conducting material used as a word line WL is thickly deposited on the whole surface, and patterns, such as a resist of the shape of a long parallel stripe, are formed on it at a line writing direction. Anisotropies, such as RIE which used this pattern as the mask, process an electrical conducting material by strong etching, and form a word line WL. Moreover, sidewall WL' of the word line WL shown in drawing 2 (B) is formed. The basic structure of a memory cell is completed by the above.

[0039] The advantage over the memory cell structure indicated by said paper in which the conventional technique of the memory cell structure concerning this operation gestalt is shown below is explained. In addition, although the case where the control gate is divided into two sidewalls in the cross-section structure indicated by the above-mentioned paper is made into the example of a comparison in the following explanation, the advantage of this invention is the same even when not dividing the control gate. Drawing 12 (A) is a sectional view in alignment with the line writing direction at the time of dividing the control gate into two further in the cross-section structure of the cel indicated by the above-mentioned paper. The top view on which drawing 12 (B) was drawn focusing on two memory cells, and drawing 13 are the top views of a memory cell array also including a control pad. In addition, in these drawings, the sign which directs the configuration which is common in this operation gestalt is unified

into what was used with this operation gestalt.
[0040] The fundamental cel configuration whose memory cell of this example of a comparison includes the point that series connection of the two memory transistors MTa and MTb is carried out to the WORD transistor WT on both sides of this is common in the memory cell of this operation gestalt.
[0041] however, the memory cell of the example of a comparison have the WORD gate WG connect to a word line WL, in the condition of having make the charge storage film CSF place between the side faces, be the point which form the sidewall-like control gates CG1, CG2, and CG3, and the point of not have the dielectric detached core ISO which perform separation between cels of the direction of a train, and differ greatly on the memory cell of this operation gestalt, and structure. The control gates CG1, CG2, and CG3 need to form at least the WORD gate WG which serves as an auxiliary layer at the time of the formation in the direction of a train in the shape of [long] an parallel stripe from the need of forming in the direction of a train for a long time. However, on the other hand, in order to separate between word lines WL electrically, it is necessary to divide the stripe-like WORD gate WG to the isolated pattern for every cel. The above point is clear on the cellular structure.
[0042] Hereafter, order is briefly described for the manufacture approach expected from the cellular structure of the example of a comparison later on. First, the laminating of the electric conduction film used as the dielectric film DF of a monolayer and the WORD gate WG is carried out on Substrate SUB, pattern NINGU of these is carried out, and the pattern of the shape of a long parallel stripe is formed in the direction of a train. All over including this pattern front face and a substrate SUB front face, the charge storage film CSF which consists of ONO film is formed. An etching protective layer is formed in required parts, such as a location of the control pads CP1, CP2, and CP3 which deposit thickly the polycrystal silicon with which the impurity was doped so that between the conductive layers used as the WORD gate WG may be embedded in this condition, for example, are shown in drawing 13 , and --, and etchback of the polycrystal silicon is carried out on the strong conditions of an anisotropy by that condition. Consequently, the sidewall which consists of polycrystal silicon in the condition of having made the charge storage film CSF placed between the both-sides sides of a conductive layer used as the WORD gate WG is formed as the control gates CG1, CG1, CG2, CG2, CG3, and CG3 and --. Moreover, the control pads CP1, CP2, and CP3 and -- are formed in coincidence. After oxidizing the front face of the sidewall (polycide Wall) which consists of polycrystal silicon by the oxidizing [thermally] method, by the ion implantation which used the conductive layer used as polycide Wall and the WORD gate WG as the mask, and used the charge storage film CSF between polycide Wall as the through film, an N type impurity is introduced into the substrate surface field between polycide Wall, and source drain field S/D is formed in it. Then, after embedding the tooth space between polycide Wall with dielectrics, such as a silicon dioxide, flattening of the front face of a dielectric is carried out so that the surface height may become equal to the height of a conductive layer which serves as the WORD gate WG mostly with polish or etchback. Although the conductive layer front face used as the WORD gate WG exposes this flattening, a polycide Wall front face is stopped with extent which is not exposed by existence of the thermal oxidation film. Then, the conductive material used as a word line WL is deposited on a flattening side, and the resist of the shape of a long parallel stripe is formed on it at a line writing direction. A conductor is etched by using a resist as a mask, and between word lines WL is separated. Moreover, etching divides the conductive layer continuously exposed to the substrate between word lines WL. Thereby, the WORD gate WG is formed by the pattern isolated for every cel.
[0043] The 1st problem of this example of a comparison is a final process, and in case it divides the conductive layer used as the WORD gate WG to the pattern for every cel, it is easy to produce the residue of polycrystal silicon. That is, polycrystal silicon tends to remain in the part where the part which originates in the cross section of a conductive layer used as the WORD gate WG being trapezoidal shape as described above, will dig a hole with a back taper-like side face in case this is divided, consequently sees from surface opening, and serves as a shadow extended far back most, i.e., the part which met the lower side of a side face as shown in drawing 12 (B), in the shape of a muscle. In order

that the residue of such polycrystal silicon may make between the WORD gates WG short-circuit electrically, this memory cell array becomes word line short [poor].
[0044] In the cellular structure concerning this operation gestalt, since it does not have the conductive layer used as the WORD gate WG, it is not necessary to divide this. Moreover, in case a word line WL is separated, on the substrate of the part which carries out etching removal, it has the side face of a forward tapered shape reflecting the control gate configuration of a sidewall form. Therefore, there is an advantage that conductive material cannot remain in this part easily.
[0045] Since the 2nd trouble of the example of a comparison does not have the dielectric detached core ISO like this operation gestalt, while repeating rewriting actuation repeatedly, it is that the field of the charge storage film CSF which adjoined the storage section becomes easy to be covered with a charge regularly. Since only impregnation is carried out and the charge (electron hole) of reversed polarity poured in for the charge with which only impregnation is performed especially in rewriting actuation, for example, elimination, is not drawn out intentionally, it tends to stop at this field gradually. Consequently, leak pass becomes easy to be made into the outside of a channel. Drawing 12 (B) shows the residual field of this charge, and the direction of leak pass.
[0046] Although the part of the charge storage film CSF which touched the channel formation field CH in drawing 2 (A) serves as the storage section with this operation gestalt, the adjoining field of the storage section has run aground on the dielectric detached core ISO. Therefore, even if this adjoining field may be regularly covered with a charge, a channel is not influenced with that charge but there is an advantage that leak pass does not arise. in addition, a dielectric detached core -- LOCOS -- when it forms by law or the STI method, since a substrate surface field is insulation-ized, it is further hard to generate leakage current.
[0047] Since it is annularly formed as the 3rd trouble of the example of a comparison for having gone around the perimeter of a conductive layer where the control gate turns into the WORD gate WG as shown in drawing 13 , it is necessary to cut two places of this control gate by the shorter side side of a conductive layer. It is because it is difficult to carry out 2-bit storage actuation efficiently if the two control gates CG 1 in 1 memory cell, and CG2, CG2, CG3 and -- cannot impress an independently different electrical potential difference.
[0048] In the cellular structure of this operation gestalt, as shown in drawing 3 , it is the two control gates CG 1 in 1 memory cell, and CG2, CG2, CG3 and -- at the formation time, and they are already separated. Therefore, with this operation gestalt, as long as the adjoining control gate CG 1, and CG1, CG2, CG2 and -- are used with this potential, the process for cutting the control gate has the advantage of being unnecessary. In addition, in order to raise the degree of freedom of serial access actuation of VG cel array, it will be necessary to cut the control gate CG 1, and CG1, CG2, CG2 and -- in drawing 3 , respectively, the cutting part of the control gate only differs from the example of a comparison and the number of the parts to cut becomes the same to control all the control gates independently.
[0049] In addition, with this operation gestalt, an auxiliary layer consists of conductive material (for example, polycrystal silicon which doped the impurity), and resistance of bit lines BL1 and BL2 and -- is reduced compared with the example of a comparison which formed the bit line only in the impurity range embedded in the semi-conductor. Moreover, with this operation gestalt, channel length of the WORD transistor WT can be made smaller than minimum line width F. Since the source and the drain of the WORD transistor WT are the channel of the memory transistors MTa and MTb, even if it makes channel length of the WORD transistor WT detailed, a punch-through cannot pose a problem easily.
[0050] The alteration of the versatility [gestalt / this / operation] in within the limits of the technical thought of this invention is possible. For example, not only polycrystal silicon but it can constitute from a conductor of amorphous silicon and others, and the auxiliary layer used as the object which forms the control gate can be constituted from a dielectric. In that case, it is necessary to embed and form a source drain field in the bottom of the dielectric detached core ISO, or to carry out the dielectric

detached core ISO to to the both sides of the storage section, and to cut on source drain field S/D. Consequently, source drain field S/D is formed in the direction of a train in the shape of [long] Rhine, and uses this source drain field S/D as a bit line.

[0051] Moreover, the charge storage film SCF of the process of drawing 9 may be formed, without forming the dielectric film DF 1 by thermal oxidation in the front face of polycrystal silicon in the process of drawing 8 . In that case, in the process of drawing 11 , although the top face of the polycrystal silicon which becomes bit lines BL1 and BL2 and -- by etching of the charge storage film SCF is exposed, since the top face of the polycrystal silicon used as this bit line also oxidizes thermally and the silicon dioxide film is formed after that in case [of the control gates CG1 and CG2 and --] a front face is oxidized thermally, the insulating demarcation membrane with a word line is fully made. By this approach, the membrane formation process of the pad layer PAD in drawing 5 and the oxidation blocking layer OS, a subsequent removal process, and the thermal oxidation process in drawing 8 are unnecessary, and there is an advantage by which that part and a process are simplified.

[0052] Furthermore, it is not limited to the sidewall configuration formed in the control gates CG1 and CG2 and the side face of the auxiliary layer (the above-mentioned explanation bit lines BL1 and BL2, --) of -- which a configuration becomes from a conductor or a dielectric. For example, as shown in drawing 14 R> 4, it is good in the control gates CG1 and CG2 and -- also considering the side face and top face of bit lines BL1 and BL2 and -- as a wrap configuration. However, this configuration is limited to the application which uses electrically the control gate belonging to a different cel on both sides of a bit line with this potential. Moreover, with this configuration, the charge storage film CSF serves as a wrap configuration inevitably in the side face and top face of bit lines BL1 and BL2 and --. In the separation process of the charge storage film CSF of drawing 1111 explained previously, the charge storage film part on a bit line is because it is protected by the control gates CG1 and CG2 and --.

[0053] Hereafter, these control gates CG1 and CG2 and the formation approach of -- are explained, referring to two examples and a drawing. The 1st approach is shown in drawing 15 - drawing 17 . This manufacture approach can be enforced by replacing at the process which shows the formation process of the control gate of the sidewall form which explains previously and is shown in drawing 10 to drawing 15 and drawing 16 .

[0054] After forming bit lines BL1 and BL2, source drain field S/D, a dielectric DF 1, and the charge storage film CSF through the same process as drawing 5 - drawing 9 , as shown in drawing 15 , the electric conduction film CGF which consists of polycrystal silicon or amorphous silicon is formed in the whole surface. Moreover, a resist pattern R1 is formed by the photolithography on the electric conduction film CGF part located on bit lines BL [BL1 and] 2.

[0055] By etching which used this resist pattern R1 as the mask, pattern NINGU of the electric conduction film CGF is carried out. Thereby, as shown in drawing 16 , the control gates CG1 and CG2 separated in the upper part of the center section of the channel formation field are formed. Etching at this time has a moderately strong anisotropy, and its conditions on which a resist pattern R1 retreats a little are desirable. It is because the edge of a resist pattern R1 retreats, consequently the main fields of the side face of the control gates CG1 and CG2 serve as a forward tapered shape in connection with a resist pattern R1 carrying out film decrease during etching. In addition, in order to easy-ize retreat of an edge, you may make it go around [the edge of a resist pattern R1] beforehand by comparatively hot postbake etc.

[0056] As shown in drawing 17 , etching which used these control gates CG1 and CG2 as the mask is performed, and the charge storage film CSF is separated. Moreover, in order to consider as the structure of drawing 14 , with having described above, by the same approach, a dielectric film DF 2 and a word line WL are formed, and the basic structure of the memory cell concerned is completed.

[0057] The 2nd approach is the approach of forming the mask layer at the time of processing of the electric conduction film CGF in self align to a substrate configuration. The 2nd approach is shown in drawing 18 - drawing 22 . This manufacture approach can be enforced by replacing at the process which

shows the formation process of the control gate of the sidewall form which explains previously and is shown in drawing 10 to drawing 18 - drawing 22 .

[0058] After forming bit lines BL1 and BL2, source drain field S/D, a dielectric DF 1, and the charge storage film CSF through the same process as drawing 5 - drawing 9 , as shown in drawing 18 , the electric conduction film CGF which consists of polycrystal silicon or amorphous silicon is formed in the whole surface. Then, the oxidation inhibition film OSF which consists of silicon nitride etc., for example is thinly formed in an electric conduction film CGF front face. Moreover, a resist is applied, after baking, etchback is carried out and a surface crevice is embedded by the resist R2.

[0059] Etching which used the resist R2 as the mask in this condition removes some oxidation inhibition film OSF located above bit lines BL1 and BL2, as shown in drawing 19 .

[0060] As the electric conduction film CGF exposed to the perimeter of the oxidation inhibition film OSF is alternatively oxidized thermally and is shown in drawing 20 after removing a resist R2, a dielectric film DF 2 is formed above bit lines BL1 and BL2. As shown in drawing 21 , the oxidation inhibition film OSF is removed.

[0061] By etching which used the dielectric film DF 2 as the mask, pattern NINGU of the electric conduction film CGF is carried out. Thereby, as shown in drawing 22 , the control gates CG1 and CG2 separated in the upper part of the center section of the channel formation field are formed. Etching at this time has a moderately strong anisotropy, and its conditions on which a dielectric film DF 2 retreats a little are desirable. Since a dielectric film DF 2 is formed by the selective oxidation which used the oxidation inhibition film OSF as the mask, as for the tip, in the edge part, thickness is thin like the so-called BAZU beak of LOCOS. Therefore, if a dielectric film DF 2 carries out film decrease during etching of the control gate, the edge of a dielectric film DF 2 will retreat in connection with it, consequently the main fields of the side face of the control gates CG1 and CG2 will serve as a forward tapered shape.

[0062] Then, etching which used these control gates CG1 and CG2 as the mask is performed, and the charge storage film CHS is separated. Moreover, in order to consider as the structure of drawing 14 , with having described above, by the same approach, a dielectric film DF 2 is formed in the side face of the control gates CG1 and CG2, a word line WL is formed, and the basic structure of the memory cell concerned is completed.

[0063]

[Effect of the Invention] According to the non-volatile semiconductor memory concerning this invention, and its manufacture approach, the process which connects a word line with a WORD gate electrode like the conventional example is unnecessary, and in case the 2nd control electrode is processed, the residue of conductive material which short-circuits between the 2nd control electrode does not occur. even when a charge uncontrollable by the direction which met the 1st control electrode to the contiguity field outside the storage section collects regularly, even if the effect of the channel on the charge is markedly alike, and it can weaken by existence of a dielectric detached core, consequently it repeats rewriting actuation, a leak property does not deteriorate. The process separated in order to already have separated both and to control this independently, when forming the 1st two control electrodes in 1 memory cell is unnecessary. when an auxiliary layer consisted of conductive material, compared with the case where a bit line is constituted only from an impurity range embedded in the semi-conductor, resistance of a bit line was markedly alike and was reduced. Moreover, when the side face and top face of an auxiliary layer were made into a wrap configuration for the 1st control electrode, resistance of the 1st control electrode was reduced compared with the sidewall form. Furthermore, even if it forms Rhine of the 2nd control electrode, and the width of face of SU **-SU with the minimum threshold value of lithography, leakage current does not increase by doubling gap of the 2nd control electrode, or channel width does not decrease, consequently the S/N ratio of a read-out signal does not fall.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] (A) is the top view of the memory cell concerning an operation gestalt. (B) is the sectional view which met the A-A line of (A).
[Drawing 2] (A) is the sectional view which met the B-B line of drawing 1 (A) in the memory cell concerning an operation gestalt. (B) is the sectional view which met the C-C line of drawing 1 (A).
[Drawing 3] In the nonvolatile memory concerning an operation gestalt, it is the top view of a memory cell array shown including the pad for the electrode drawers of the control gate.
[Drawing 4] It is the sectional view expanding and showing a part for the principal part of the memory cell of drawing 1 (A) concerning an operation gestalt.
[Drawing 5] In manufacture of the memory cell concerning an operation gestalt, it is a sectional view after membrane formation of a sacrifice layer.
[Drawing 6] In manufacture of the memory cell concerning an operation gestalt, it is the sectional view after carrying out opening of the pattern of a bit line to a sacrifice layer etc.
[Drawing 7] In manufacture of the memory cell concerning an operation gestalt, it is a sectional view after bit line formation.
[Drawing 8] In manufacture of the memory cell concerning an operation gestalt, it is the sectional view after oxidizing the front face of a bit line thermally.
[Drawing 9] In manufacture of the memory cell concerning an operation gestalt, it is the sectional view after forming the charge storage film.
[Drawing 10] In manufacture of the memory cell concerning an operation gestalt, it is a sectional view after control gate formation.
[Drawing 11] In manufacture of the memory cell concerning an operation gestalt, it is a sectional view after removing some charge storage film which used the control gate as the mask.
[Drawing 12] (A) is the outline sectional view showing the structure of the memory cell concerning the example of a comparison of an operation gestalt. (B) is the top view of the memory cell array centering on two memory cells concerning the example of a comparison of an operation gestalt.
[Drawing 13] It is the top view of a memory cell array and a control pad concerning the example of a comparison of an operation gestalt.
[Drawing 14] It is the sectional view showing the modification of the control gate configuration of an operation gestalt which met the A-A line of drawing 1 (A).
[Drawing 15] It is a sectional view after formation of a resist pattern about the 1st approach of forming the control gate of a modification.
[Drawing 16] It is a sectional view after etching of the control gate about the 1st approach of forming the control gate of a modification.
[Drawing 17] It is a sectional view after etching of the charge storage film about the 1st approach of forming the control gate of a modification.
[Drawing 18] It is the embedded backward sectional view of a resist about the 2nd approach of forming the control gate of a modification.
[Drawing 19] the 2nd approach of forming the control gate of a modification -- being related -- some

oxidation inhibition film -- it is a sectional view after removal.
[Drawing 20] It is a sectional view after formation of a dielectric film about the 2nd approach of forming the control gate of a modification.
[Drawing 21] It is a sectional view after removal of the remaining oxidation inhibition film about the 2nd approach of forming the control gate of a modification.
[Drawing 22] It is a sectional view after etching of the control gate about the 2nd approach of forming the control gate of a modification.
[Description of Notations]
MTa, MTb -- A memory transistor, WT -- WORD transistor, WL, WL1, WL2, WL3 -- A word line (the 2nd control electrode), WL' -- Sidewall, BL1, BL2, BL3 -- A bit line, CG1, CG21, CG3 -- Control gate (the 1st control electrode), ISO -- A dielectric detached core, SUB -- A substrate (semi-conductor), S/D -- Source drain field (impurity range), CH -- A channel formation field, DF1 -- A dielectric film, DF2 -- The dielectric film of a monolayer, CSF -- The charge storage film, CP1, CP2, CP3 -- Control pad (drawer field of the 1st control electrode), BTM [-- A pad layer, OS / -- An oxidation blocking layer, SF / -- A sacrifice layer, WG / -- The WORD gate, OSF / -- The oxidation inhibition film, R1, R2 / -- Resist.] -- The bottom film, CS -- The middle charge storage film, TOP -- The top film, PAD

[Translation done.]

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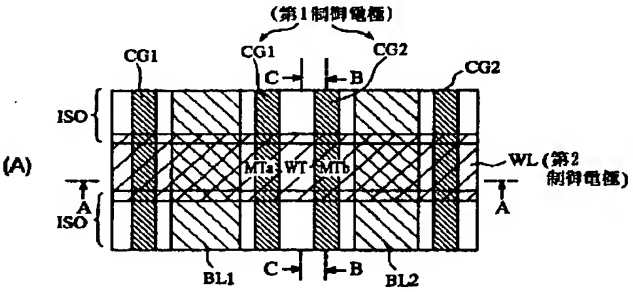
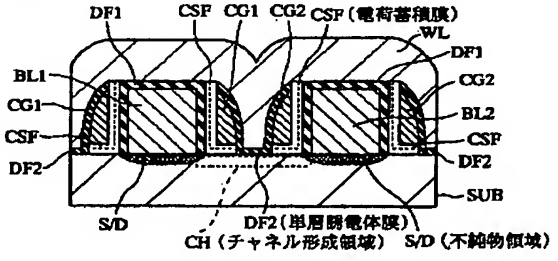
最終頁に続く

(54)【発明の名称】　不揮発性半導体記憶装置およびその製造方法

(57)【要約】
【課題】ワード線間を短絡するような導電性残渣の発生を防止する。
【解決手段】メモリセルが、チャネル形成領域ＣＨと、積層された複数の誘電体膜からなる電荷蓄積膜ＣＳＦと、チャネル形成領域ＣＨの両端部上に重なる電荷蓄積膜ＣＳＦの領域からなる２つの記憶部と、記憶部間でチャネル形成領域ＣＨ上に接した単層の誘電体膜ＤＦ２と、２つの不純物領域Ｓ／Ｄ上に各々形成された補助層（たとえばビット線ＢＬ１，ＢＬ２）と、補助層に誘電体膜を介在させて形成され記憶部上に位置する２つの第１制御電極ＣＧ１，ＣＧ２と、その間のスペースに第１制御電極ＣＧ１，ＣＧ２と絶縁された状態で埋め込まれ、かつ単層の誘電体膜ＤＦ２上に接した第２制御電極ＷＬとを有している。第１制御電極ＣＧ１，ＣＧ２の対向面の主な領域は順テーパとなるため第２制御電極ＷＬの加工時に導電性の残渣が残らない。



(B) A-A断面



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【特許請求の範囲】

【請求項１】メモリセルを有し、

当該メモリセルが、半導体からなるチャネル形成領域と、

積層された複数の誘電体膜からなり電荷保持能力を有した電荷蓄積膜と、

上記チャネル形成領域の両端部上に重なる上記電荷蓄積膜の領域からなる２つの記憶部と、

上記記憶部間で上記チャネル形成領域上に接した単層の誘電体膜と、

互いに対向する面の主な領域が順テーパ状となるように上記記憶部の各々の上に１つずつ形成された２つの第１制御電極と、

上記２つの第１制御電極間のスペースに各第１制御電極と絶縁された状態で埋め込まれ、かつ上記単層の誘電体膜上に接した第２制御電極とを有した不揮発性半導体記憶装置。

【請求項２】上記メモリセルが、上記チャネル形成領域と逆導電型の半導体からなりチャネル形成領域を挟んで互いに離間する２つの不純物領域と、

上記２つの不純物領域上に各々形成され、上記第１制御電極の、上記メモリセルの外側に面したそれぞれの面に近接した２つの補助層とをさらに有した請求項１記載の不揮発性半導体記憶装置。

【請求項３】上記補助層は、誘電体膜を介在させた状態で上記第１制御電極の外側面に近接した導電層からなる請求項２記載の不揮発性半導体記憶装置。

【請求項４】上記導電層は、上記不純物領域と同じ導電型の不純物が導入された多結晶珪素または非晶質珪素の層からなる請求項３記載の不揮発性半導体記憶装置。

【請求項５】上記補助層は、上記第１制御電極の外側面に近接した誘電体層からなる請求項２記載の不揮発性半導体記憶装置。

【請求項６】上記チャネル形成領域、上記２つの記憶部、上記第１および第２制御電極、上記２つの補助層および上記２つの不純物領域を有したメモリセルが行列状に複数配置されてメモリセルアレイが構成され、

上記２つの補助層のそれぞれが、列方向に長く配置されて複数のメモリセルで共有され、かつ行方向に隣接した２つのメモリセルで共有され、

上記２つの第１制御電極が、上記２つの補助層に沿って配置されて複数のメモリセルで共有され、

上記第２制御電極が、行方向に長く配置されて複数のメモリセルで共有された請求項２記載の不揮発性半導体記憶装置。

【請求項７】行方向に隣接した２つのメモリセルで共有された上記補助層を幅方向両側から挟む２つの上記第１制御電極が電気的に導通している請求項６記載の不揮発性半導体記憶装置。

【請求項８】上記第１制御電極が、上記補助層の幅方向

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両側に形成されたサイドウォール形状の導電層からなり、

上記サイドウォール形状を有した２つの第１制御電極が、上記メモリセルアレイの外側で互いに接続された請求項７記載の不揮発性半導体記憶装置。

【請求項９】上記第１制御電極は、上記補助層の２つの側面と上面とを覆う導電層からなる請求項７記載の不揮発性半導体記憶装置。

【請求項１０】列方向に隣接したメモリセル間で上記チャネル形成領域を電気的に分離する誘電体分離層が、少なくとも上記第２制御電極間の上記半導体の表面領域に形成された請求項６記載の不揮発性半導体記憶装置。

【請求項１１】上記第２制御電極は、その幅方向両側にサイドウォールを有し、

当該サイドウォールのそれぞれが上記誘電体分離層の縁部上に重なった請求項１０記載の不揮発性半導体記憶装置。

【請求項１２】複数のメモリセルを有し、

各メモリセルが、

第１導電型半導体からなるチャネル形成領域と、

第２導電型半導体からなり上記チャネル形成領域を挟んで互いに離間した第１および第２不純物領域と、

上記第１および第２不純物領域の離間方向と直交する方向に長く配置されて複数のメモリセルで共有された制御電極と、

上記制御電極の直ぐ下の層に形成された複数の誘電体膜からなり、上記チャネル形成領域上に重なった部分に情報を記憶する電荷蓄積膜とを有し、

上記第１および第２不純物領域の離間方向と直交する方向に隣接するメモリセルが誘電体分離層によって電気的に分離され、

上記誘電体分離層によって分離された上記隣接メモリセルの上記第１不純物領域同士および上記第２不純物領域同士が、それぞれ導電層により接続された不揮発性半導体記憶装置。

【請求項１３】第１導電型半導体からなるチャネル形成領域と、上記チャネル形成領域を挟んで離間し第２導電型半導体からなる２つの不純物領域と、上記２つの不純物領域に近い上記チャネル形成領域の両端部上に複数の誘電体膜からなる電荷蓄積膜を介在させた状態で形成された２つの第１制御電極と、第１制御電極間の上記チャネル形成領域上に単層の誘電体膜を介在させた状態で対面し、上記不純物領域の離間方向に長く配置された第２制御電極とを有した不揮発性半導体記憶装置の製造方法であって、

上記製造方法が以下の諸工程、すなわち、

上記不純物領域の離間方向と直交する方向に長いライン形状を有した補助層を上記不純物領域上または上記不純物領域が形成される半導体領域上に形成し、

上記補助層の表面と上記チャネル形成領域の表面との上

に上記電荷蓄積膜を形成し、
上記電荷蓄積膜を介在させた状態で上記補助層に沿って上記第１制御電極を形成し、
上記第１制御電極をマスクとしたエッチングにより電荷蓄積膜の一部を除去し、
上記電荷蓄積膜の除去により露出した上記チャネル形成領域の表面と上記第１制御電極の表面とに単層の誘電体膜を形成し、
上記単層の誘電体膜と上記補助層との上に上記第２制御電極を形成する各工程を含む不揮発性半導体記憶装置の製造方法。
【請求項１４】上記補助層は、誘電体層からなる請求項１３記載の不揮発性半導体記憶装置の製造方法。
【請求項１５】上記補助層は、導電層からなる請求項１３記載の不揮発性半導体記憶装置の製造方法。
【請求項１６】上記補助層は、第２導電型不純物が導入された多結晶珪素または非晶質珪素からなる請求項１５記載の不揮発性半導体記憶装置の製造方法。
【請求項１７】上記補助層を拡散源とした固相拡散により上記第２導電型の不純物領域を形成する工程をさらに含む請求項１６記載の不揮発性半導体記憶装置の製造方法。
【請求項１８】上記第２制御電極と上記補助層との間を絶縁するために、上記補助層をなす多結晶珪素または非晶質珪素の表面を選択的に熱酸化する工程をさらに含む請求項１６記載の不揮発性半導体記憶装置の製造方法。
【請求項１９】上記補助層の形成工程が以下の諸工程、すなわち、
パッド酸化膜、窒化膜および犠牲層をこの順で積層して積層膜を形成し、
上記積層膜の一部をエッチングにより除去し、
第２導電型不純物が導入された多結晶珪素または非晶質珪素を上記積層膜の除去した部分に埋め込んで上記補助層を形成し、
上記犠牲層を除去し、
上記窒化膜を酸化阻止膜として上記多結晶珪素または非晶質珪素の表面を熱酸化する各工程を含む請求項１８記載の不揮発性半導体記憶装置の製造方法。
【請求項２０】上記多結晶珪素または非晶質珪素の表面を熱酸化する際に、上記多結晶珪素または非晶質珪素を拡散源とした固相拡散により第２導電型の上記不純物領域を形成する請求項１９記載の不揮発性半導体記憶装置の製造方法。
【請求項２１】上記補助層の形成工程が以下の諸工程、すなわち、
上記補助層のパターンにて上記積層膜に開口部を形成し、
上記開口部を通して第２導電型不純物を導入して、上記開口部底面に露出する半導体領域に第２導電型の上記不純物領域を形成し、

不純物が導入された多結晶珪素または非晶質珪素を上記開口部内に埋め込む各工程をさらに含む請求項１９記載の不揮発性半導体記憶装置の製造方法。
【請求項２２】上記第１制御電極の形成工程では、導電膜を堆積しエッチバックすることにより上記補助層の幅方向両側にサイドウォール形状の第１制御電極を形成する請求項１３記載の不揮発性半導体記憶装置の製造方法。
【請求項２３】上記第１制御電極の形成工程が、
導電膜を堆積し、
上記補助層の上方に位置する導電膜上にエッチング保護層を形成し、
補助層の上方部分をエッチング保護層により保護しながら上記導電膜をエッチングし、上記チャネル形成領域の中央部の上方に位置する部分で上記導電膜を分離する各工程をさらに含む請求項１３記載の不揮発性半導体記憶装置の製造方法。
【請求項２４】上記エッチング保護層の形成工程が、
上記補助層の形状を反映してできた上記導電膜の凹部の内壁に酸化阻止膜を形成し、
酸化阻止膜に覆われていない上記補助層の上方に位置する導電膜部分の表面を熱酸化して上記エッチング保護層を形成し、
上記酸化阻止膜を除去する各工程をさらに含む請求項２３記載の不揮発性半導体記憶装置の製造方法。
【請求項２５】一方向に長い平行ライン状の誘電体分離層を第１導電型の半導体に形成し、不純物が導入された多結晶珪素または非晶質珪素からなる補助層を、上記誘電体分離層と直交する方向に長い平行ライン状に形成し、
上記誘電体分離層の間で上記補助層の配置領域と重なる半導体箇所に、第２導電型の上記不純物領域を形成する各工程をさらに含む請求項１３記載の不揮発性半導体記憶装置の製造方法。
【請求項２６】上記第１制御電極を形成する工程が以下の諸工程、すなわち、
上記第１制御電極となる導電膜を堆積し、
上記第１制御電極の引き出し領域となる導電膜部分の上にエッチング保護層を形成し、
上記導電膜をエッチバックする各工程を含む請求項１３記載の不揮発性半導体記憶装置の製造方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、チャネル形成領域の両端部に、複数の誘電体膜を積層させた電荷蓄積膜からなる２つの記憶部を有し、当該記憶部に対し２ビット情報を独立に記憶可能な不揮発性半導体記憶装置と、その製造方法とに関する。
【０００２】
【従来の技術】従来より、いわゆるＭＯＮＯＳ(Metal-O

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xide-Nitride-Oxide-Semiconductor)型など、複数の誘電体膜を積層させた電荷蓄積膜を有し、この電荷蓄積膜内の電荷トラップに蓄積する電荷量を制御することで情報の記憶を行う不揮発性半導体記憶素子が知られている。

【０００３】最近になって、従来のＣＨＥ(Channel Hot Electron)注入方式によって電荷を離散的な電荷トラップの分布領域の一部に注入できることに注目して、電荷蓄積膜のソース側とドレイン側に２値情報を独立に書き込むことにより、１メモリセル当たり２ビットを独立に記憶可能な技術が報告された。

【０００４】たとえば“2000 Symposium on VLSI Technology, pp.122-123”では、ソース側とドレイン側に電荷蓄積膜を分離して設け、電荷蓄積膜上に制御電極を設け、かつ、制御電極間のチャネル中央部に電荷保持能力を有しない単層の誘電体膜を介在させた状態でワードゲート電極を設けている。ワードゲート電極はワード線に接続され、制御電極はワード線と直交する方向に配線されて、ワードゲート電極とは独立に制御される。このため、電荷注入の位置の制御性および電荷注入効率を上げることができ、その結果、高速書き込みを達成している。

【０００５】このメモリセルはツインＭＯＮＯＳセルと称せられ、行方向に一定間隔で繰り返したワードゲート電極を有し、その行方向両側の壁面にサイドウォール形の導電層を有している。このサイドウォール形の導電層の直下にＯＮＯ(Oxide-Nitride-Oxide)膜、すなわち電荷保持能力を有した電荷蓄積膜を有している。これに対し、ワードゲート電極の直下には単層の誘電体膜が形成され、そのため、この部分は電荷保持能力を有しない。サイドウォール形の導電層とワードゲート電極をマスクとして、隣接するサイドウォール形の導電層間に表出する基板箇所にＮ型不純物を導入し、ソースまたはドレインとなるN^+不純物領域を形成している。

【０００６】

【発明が解決しようとする課題】前記した論文には具体的な製造方法は開示されていないが、このツインＭＯＮＯＳセルは、以下に示す製造上および構造上の問題点がある。

【０００７】このツインＭＯＮＯＳセルでは、ワードゲート電極を形成した後、その側面にサイドウォール形の導電層を形成する。そのため、その後、ワードゲート電極をワード線と接続する工程が必要である。

【０００８】また、このツインＭＯＮＯＳセルにおけるワードゲート電極は、最初は、列方向に長い平行ライン状にパターンニングする必要がある。このとき、通常、ワードゲート電極材料を堆積した後、その上にレジストのパターンを形成し、このレジストをマスクとして異方性が強いエッチング方法、たとえばＲＩＥ(Reactivelon Etching)によりワードゲート電極材料を加工する。レ

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ジストパターンの断面形状は側面が順テーパとなるのが普通であり、またエッチング時のレジストが多少なりとも後退するため、加工後のワードゲート電極の側面も順テーパとなる。また、レジストを用いないでエッチング時に後退しない材料を用いても、エッチング時の側壁付着物の影響等により、加工後のワードゲート電極の側面に多少なりとも順テーパが出来やすい。このワードゲート電極は、その後、たとえばワード線をパターンニングする際に同時に加工しセル間で分離する必要がある。ところが、このとき既にワードゲート電極の側壁に対し絶縁膜を介在させた状態で制御電極が形成されているため台形状の断面形状を有した穴を掘りながら、ワードゲート電極を選択的にエッチングにより除去しなければならない。したがって、このエッチング時に逆テーパ状の制御電極の側面の下部側がエッチングされ難く、この部分に制御電極に沿って導電性の残渣が生じやすい。導電性の残渣が生じると、ワード線間のショート不良となる。

【０００９】また、サイドウォール形の導電層は、ワードゲート電極となるライン状の導電層の周囲を一周して環状に形成される。このままサイドウォール形の導電層を制御電極とすると、ソース側の制御電極とドレイン側の制御電極は電気的に短絡した状態となる。したがって、ソース側の制御電極とドレイン側の制御電極とに異なる電圧を印加するには、両制御電極を分離しなければならない。この分離は他の工程、たとえばワード線加工時に一括して行うことができないため、たとえばワードゲート電極となるライン状の導電層の両端部側のみ開口したエッチングマスクを形成し、この開口部を通してサイドウォール形の導電層を覆う絶縁膜を除去してから導電層をエッチングにより切断する工程が必要となる。

【００１０】さらに、ツインＭＯＮＯＳセルではサイドウォール形の導電層の直下にＯＮＯ膜を形成しているため、チャネル形成領域に接するＯＮＯ膜は、サイドウォール形の導電層に沿って列方向に長く延びている。動作時に、チャネルと交差するＯＮＯ膜領域（以下、記憶部という）に電荷を注入して書き込みが行われ、また、この記憶部に対し、蓄積電荷を基板側に引き抜いたり逆導電型の電荷を注入することによって消去が行われる。この書き換え動作を何度も繰り返すうちに、記憶部の隣接領域に電荷が定常的に溜まりやすくなる。そして、この電荷によってチャネルの外側にリークパスができやすくなる。蓄積された電荷を電子でチャネル全面から引き抜いて消去する場合は、記憶部と同様に、その隣接領域も制御電極の支配下にあり、隣接領域に溜まった電子も同時に引き抜きかれるので余り問題とならない。ところが、とくに蓄積された電荷を消去するするため逆極性の電荷を記憶部に注入する場合に、チャネルをオンする方向の極性をもった電荷、たとえばＮ型チャネルの場合の正孔が記憶部の隣接領域に溜まるとリークパスが生じやすくなるため、これによるリーク特性の低下が問題とな

る。

【００１１】本発明の第１の目的は、ワードゲート電極をワード線（第２制御電極）と一体として形成することを構造上可能にすることによって、ワードゲート電極とワード線を接続する工程を不要とすることにある。本発明の第２の目的は、ワード線間を短絡するような導電性残渣の発生を防止し、また、同一セル内の２つの制御電極間を切断するための工程を構造上不要にすることにある。本発明の第３の目的は、記憶部に対し制御電極に沿った方向の隣接領域あるいは記憶部間に不要な電荷が溜まることを防止し、リーク電流が発生しない構造とすることにある。

【００１２】

【課題を解決するための手段】上記第１および第２の目的を達成するために、本発明の第１の観点に係る不揮発性半導体記憶装置は、メモリセルを有し、当該メモリセルが、半導体からなるチャネル形成領域と、積層された複数の誘電体膜からなり電荷保持能力を有した電荷蓄積膜と、上記チャネル形成領域の両端部上に重なる上記電荷蓄積膜の領域からなる２つの記憶部と、上記記憶部間で上記チャネル形成領域上に接した単層の誘電体膜と、互いに対向する面の主な領域が順テーパ状となるように上記記憶部の各々の上に１つずつ形成された２つの第１制御電極と、上記２つの第１制御電極間のスペースに各第１制御電極と絶縁された状態で埋め込まれ、かつ上記単層の誘電体膜上に接した第２制御電極とを有している。また、上記メモリセルが、上記チャネル形成領域と逆導電型の半導体からなりチャネル形成領域を挟んで互いに離間する２つの不純物領域と、上記２つの不純物領域上に各々形成され、上記第１制御電極の、上記メモリセルの外側に面したそれぞれの面に近接した２つの補助層とをさらに有している。

【００１３】上記補助層は、好適に、誘電体膜を介在させた状態で上記第１制御電極に近接し、導電層もしくは、上記不純物領域と同じ導電型の不純物が導入された多結晶珪素または非晶質珪素の層からなる。あるいは、上記補助層は、上記第１制御電極に近接した誘電体層からなる。

【００１４】複数のメモリセルを行列状に配置した構成において、行方向に隣接した２つのメモリセル間で共有された上記補助層を幅方向両側から挟む２つの上記第１制御電極は、その形状をサイドウォール形としてもよいし、補助層の上方で互いに接続された形状としていもよい。後者の形状の第１制御電極は、上記補助層の２つの側面と上面とを覆う導電層からなり、サイドウォール形と比べて配線抵抗が低い。

【００１５】上記第３の目的を達成するために、本発明の第２の観点に係る不揮発性半導体記憶装置は、複数のメモリセルを有し、各メモリセルが、第１導電型半導体からなるチャネル形成領域と、第２導電型半導体からなり上記チャネル形成領域を挟んで互いに離間した第１および第２不純物領域と、上記第１および第２不純物領域の離間方向と直交する方向に長く配置されて複数のメモリセルで共有された制御電極と、上記制御電極の直ぐ下の層に形成された複数の誘電体膜からなり、上記チャネル形成領域上に重なった部分に情報を記憶する電荷蓄積膜とを有し、上記第１および第２不純物領域の離間方向と直交する方向に隣接するメモリセルが誘電体分離層によって電気的に分離され、上記誘電体分離層によって分離された上記隣接メモリセルの上記第１不純物領域同士および上記第２不純物領域同士が、それぞれ導電層により接続されている。

【００１６】上記第１および第２の目的を達成するために、本発明の第３の観点に係る不揮発性半導体記憶装置の製造方法は、第１導電型半導体からなるチャネル形成領域と、上記チャネル形成領域を挟んで離間し第２導電型半導体からなる２つの不純物領域と、上記２つの不純物領域に近い上記チャネル形成領域の両端部上に複数の誘電体膜からなる電荷蓄積膜を介在させた状態で形成された２つの第１制御電極と、上記第１制御電極間の上記チャネル形成領域上に単層の誘電体膜を介在させた状態で対面し、上記不純物領域の離間方向に長く配置された第２制御電極とを有した不揮発性半導体記憶装置の製造方法であって、上記製造方法が以下の諸工程、すなわち、上記不純物領域の離間方向と直交する方向に長いライン形状を有した補助層を上記不純物領域上または上記不純物領域が形成される半導体領域上に形成し、上記補助層の表面と上記チャネル形成領域の表面との上に上記電荷蓄積膜を形成し、上記電荷蓄積膜を介在させた状態で上記補助層に沿って上記第１制御電極を形成し、上記第１制御電極をマスクとしたエッチングにより電荷蓄積膜の一部を除去し、上記電荷蓄積膜の除去により露出した上記チャネル形成領域の表面と上記第１制御電極の表面とに単層の誘電体膜を形成し、上記単層の誘電体膜と上記補助層とに上記第２制御電極を形成する各工程を含む。

【００１７】上記第３の目的を達成するために、前記した第３の観点に係る不揮発性半導体記憶装置の製造方法において、一方向に長い平行ライン状の誘電体分離層を第１導電型の半導体に形成し、不純物が導入された多結晶珪素または非晶質珪素からなる補助層を、上記誘電体分離層と直交する方向に長い平行ライン状に形成し、上記誘電体分離層の間で上記補助層の配置領域と重なる半導体箇所に、第２導電型の上記不純物領域を形成する各工程をさらに含む。

【００１８】本発明の第１の観点に係る不揮発性半導体記憶装置、および第３の観点に係る不揮発性半導体記憶装置の製造方法によれば、１メモリセルを構成する２つの第１制御電極の対向面の主な領域が順テーパ状となるため、第２制御電極を加工する際に、第２制御電極間を

ショートするような導電物質の残渣が発生しない。また、第２制御電極を加工するだけでワード線の形成が終了する。本発明の第２の観点に係る不揮発性半導体記憶装置によれば、記憶部となる電荷蓄積膜部分に対し第１制御電極の長手方向両側に隣接した電荷蓄積膜の領域が、チャネル形成領域間の誘電体分離層上に乗り上げている。誘電体分離層の厚さをたとえば数十ｎｍ程度とするだけで、この隣接領域に電荷が蓄積された場合でも、その電荷の、誘電体分離層直下の半導体に対する影響が従来より格段に弱められる。

【００１９】

【発明の実施の形態】以下、本発明の実施の形態を、Ｎ型チャネルのメモリセルを用い、メモリセルアレイ方式がＶＧ(Vertual Ground)型の不揮発性メモリを例として、図面を参照しながら説明する。図１（Ａ）はメモリセルの平面図であり、図１（Ｂ）は図１（Ａ）のＡ－Ａ線に沿った断面図である。また、図２（Ａ）は図１（Ａ）のＢ－Ｂ線に沿った断面図、図２（Ｂ）は図１（Ａ）のＣ－Ｃ線に沿った断面図である。

【００２０】これらの図において、符号ＳＵＢは、Ｐ型の半導体基板、Ｐ型のウエルまたはＳＯＩ(Silicon On Insulator)層などＰ型の各種の半導体層を示している。便宜上、以下、基板ＳＵＢという。基板ＳＵＢ上に、図の横方向（行方向）に長い平行ストライプ状の誘電体分離層ＩＳＯが形成されている。誘電体分離層ＩＳＯは、ＬＯＣＯＳ(Local Oxidation of Silicon)法、ＳＴＩ(Shallow Trench Isolation)法あるいはフィールドアイソレーション(Field Isolation) 法の何れかによって形成される。ここでは、フィールドアイソレーション法が採用され、数１０ｎｍ程度の厚さの誘電体膜（誘電体分離層ＩＳＯ）が基板ＳＵＢ上に形成されている。この誘電体分離層ＩＳＯ間の行方向に長いライン状の領域が、当該メモリセルの半導体活性領域である。

【００２１】半導体活性領域内で、所定間隔をおいて、Ｎ型不純物が導入されたソース・ドレイン領域Ｓ／Ｄが形成されている。ソース・ドレイン領域Ｓ／Ｄ間の半導体活性領域がトランジスタのチャネル形成領域ＣＨである。Ｎ型不純物が高濃度に導入された多結晶珪素からなるビット線ＢＬ１，ＢＬ２が、行方向と直交する図の縦方向（列方向）に長い平行ライン状のパターンにて形成されている。ビット線ＢＬ１，ＢＬ２は、誘電体分離層ＩＳＯ上を横切りながら、列方向のメモリセルのソース・ドレイン領域Ｓ／Ｄ上に接触し、これらのメモリセルに共通のソース電圧またはドレイン電圧を供給する。ビット線ＢＬ１，ＢＬ２を構成する多結晶珪素の厚さは、たとえば１００ｎｍ～５００ｎｍ程度である。この多結晶珪素の表面は、誘電体膜ＤＦ１により覆われている。

【００２２】複数の誘電体膜からなる電荷蓄積膜ＣＳＦが、このビット線ＢＬ１，ＢＬ２の側面の誘電体膜ＤＦ１とチャネル形成領域の端部上とに接した状態で形成されている。電荷蓄積膜ＣＳＦは断面Ｌ字形状を有し、その底部上にサイドウォール形状の第１制御電極（以下、制御ゲートという）ＣＧ１，ＣＧ２が形成されている。制御ゲートＣＧ１，ＣＧ２は、電荷蓄積膜ＣＳＦとともにビット線ＢＬ１，ＢＬ２に沿って列方向に長く配置されている。制御ゲートＣＧ１，ＣＧ２は、詳細は後述するが、たとえば、ビット線ＢＬ１，ＢＬ２の表面を誘電体膜ＤＦ１および電荷蓄積膜ＣＳＦで覆った状態で多結晶珪素の膜を堆積し、これをエッチバックすることにより形成される。制御ゲートＣＧ１，ＣＧ２は、ビット線ＢＬ１，ＢＬ２の側面に誘電体膜を介在させた状態で支持されている。したがって、ビット線ＢＬ１，ＢＬ２は、制御ゲートＣＧ１，ＣＧ２に対しては“補助層”として機能する。また、制御電極ＣＧ１，ＣＧ２とチャネル形成領域ＣＨとに挟まれた電荷蓄積膜部分、すなわち電荷蓄積膜ＣＳＦの底部が、電荷が注入蓄積されて情報の記憶が行われる“記憶部”となる。

【００２３】制御ゲートＣＧ１，ＣＧ２間の対向面の主な領域が順テーパとなっている。この対向面が順テーパとなっていることの利点は後述する。制御ゲートＣＧ１，ＣＧ２の対向面上およびチャネル形成領域ＣＨ上に、単層の誘電体膜ＤＦ２が形成されている。この制御ゲート間の空間を埋める導電物質により、ワード線ＷＬが形成されている。ワード線ＷＬは、ビット線ＢＬ１，ＢＬ２上の誘電体膜ＤＦ１上を横切りながら半導体活性領域とほぼ同じパターンにて形成されている。また、ワード線ＷＬの幅方向両側の側面に、導電物質からなるサイドウォールＷＬ’が形成されている。

【００２４】サイドウォールＷＬ’を設けた理由は、次の通りである。列方向のセルサイズを最小にするには、誘電体分離層ＩＳＯのラインとスペース、ワード線ＷＬのラインとスペースを、ともにフォトリソグラフィの解像限界等で決まる最小線幅Ｆで形成することが望ましい。その場合、必然的に、誘電体分離層ＩＳＯのスペース幅である半導体活性領域の幅は、ワード線ＷＬの幅とほぼ一致し、両者の間に合わせ余裕がとれなくなる。したがって、図２（Ｂ）に示す制御ゲートＣＧ１，ＣＧ２間の対向スペースにおいて、半導体活性領域（チャネル形成領域ＣＨ）に対し、ワード線ＷＬが幅方向にずれると、チャネル形成領域ＣＨの一部でワード線ＷＬに重ならない領域ができてしまう。この領域はワード線ＷＬによる電界の支配を受けないため、ソースとドレイン間のリークパスとなり、その結果、チャネルをオフ状態にすることができなくなる。とくに、ワード線が幅方向にずれることによって、記憶部端にホットエレクトロンが注入されない領域が出来る。ところがホットホール注入を用いて消去を行う場合、この記憶部端は制御ゲートの電界支配下にあるためホットホールが注入され、その直下の半導体部分のしきい値電圧のみが大きく低下し、そこを通してリーク電流が増大してしまう。また、ワード線

WLの位置ずれによってチャネル幅が減少するという問題がある。ワード線幅の減少は読み出し電流の低下につながり、リーク電流の増大と相まって、読み出し信号のS／N比の低下を加速するという不利益をともなう。本実施形態では、ワード線WLの側面に、ワード線WLの幅を実質的に拡張するサイドウォールWL'を設けることにより、ワード線WLを最小線幅Fで形成しながらも上記したリークパスの形成およびチャネル幅の減少を防止することが可能となる。なお、この目的を達成するために、サイドウォールWL'の幅はフォトリソグラフィの合わせ余裕と同じか、それ以上必要である。また、この目的を達成するためには、ワード線WLを加工する際に、その下地の誘電体膜DF2まで連続してエッチングしないことが重要となる。なぜなら、誘電体膜DF2がチャネル形成領域CHの表面を完全に覆っていないと、図2（B）においてワード線WLが幅方向にずれた場合にサイドウォールWL'が直接チャネル形成領域CHの表面に接触してしまうことから、このような事態を避けるためである。

【0025】このような構成のメモリセルにおいては、ワード線WLをゲートとする中央のワードトランジスタWTと、ワードトランジスタWTを挟んで両側に位置し制御ゲートCG1またはCG2をゲートとする2つのメモリトランジスタMTa，MTbとが直列接続されて形成されている。すなわち、動作時に、ワードトランジスタWTを、2つのメモリトランジスタMTa，MTbのチャネルをソースとドレインとして機能させ、メモリトランジスタMTa，MTbを、ソース・ドレイン領域S／Dの何れか一方とワードトランジスタWTのチャネルとをソースとドレインとして機能させる。

【0026】図3は、制御ゲートの電極引き出し用のパッドを含めて示すメモリセルアレイの平面図である。この図示例は、ビット線両側の制御ゲートCG1同士、制御ゲートCG2同士、および制御ゲートCG3同士を同電位で制御する制御方法に対応する。本実施形態では、制御ゲートがビット線の周囲に形成されるサイドウォール形の導電層からなるため、1つのメモリセル内における2つの制御ゲート、すなわち制御ゲートCG1とCG2、あるいは制御ゲートCG2とCG3は、制御ゲート形成時に既に分離されている。したがって、1つのメモリセル内における2つの制御ゲートを切断する必要がない。

【0027】制御パッドCP1，CP2，CP3を形成するには、制御ゲート形成時に、制御ゲートとなる導電膜を堆積した後、制御パッドCP1，CP2，CP3を形成する領域に面積の大きな矩形パターンのエッチング保護層を形成し、その後、エッチバックを行う。エッチバック後にエッチング保護層を除去すると、その部分に制御パッドCP1，CP2，CP3が残される。図3は、環状の制御ゲートの短辺に接続するように制御パッドを形成した例である。なお、行方向のメモリセル間でシリアルアクセスの自由度を高めるために、隣接するセル間で制御ゲートに独立に異なる電圧を印加させたい場合は、ビット線両側の制御ゲートを切断する工程が必要となり、また、切断した制御ゲートに対し個々に制御パッドの形成が必要となる。

【0028】図4は、メモリセルの主要部分を拡大して示す断面図である。この図4に示すように、電荷蓄積膜CSFは、たとえば3層の誘電体膜から構成される。最下層のボトム膜BTMおよび最上層のトップ膜TOPは、たとえば、二酸化珪素、酸化窒化珪素(silicon oxynitride)または電荷トラップが少ない窒化珪素などからなる。ボトム膜BTMは基板との間で電位障壁として機能し、トップ膜TOPは、蓄積電荷がゲート側に抜けたり不要な電荷がゲート側から電荷が入ることを防止する膜として機能する。中間の膜CSには電荷トラップが多く含まれ、主として電荷蓄積を担う膜として機能する。中間の膜CSは、電荷トラップを多く含む窒化珪素や酸化窒化珪素、あるいは金属酸化物からなる絶縁性物質（誘電体）などにより構成される。

【0029】書き込み時に、記憶部1に電荷注入を行う場合は、ビット線BL1に正のドレイン電圧、ビット線BL2に基準電圧を印加し、制御ゲートCG1，CG2に個別に最適化された正電圧を印加し、ワード線WLにチャネルを形成する程度の正電圧を印加する。このとき、ビット線BL2に接続されたソース・ドレイン領域S／Dからチャネルに供給された電子がチャネル内を加速され、ビット線BL1に接続されたソース・ドレイン領域S／D側で高いエネルギーを得て、ボトム膜BTMの電位障壁を越えて記憶部1に注入され、蓄積される。記憶部2に電荷を注入する場合は、制御ゲートCG1，CG2間の電圧を切り替え、かつビット線BL1，BL2間の電圧を切り替える。これにより、電子の供給側と電子がエネルギー的にホットになる側が上記の場合と反対となり、電子が記憶部2に注入される。

【0030】読み出し時には、読み出し対象のビットが書き込まれた記憶部側がソースとなるようにビット線BL1，BL2間に所定の読み出しドレイン電圧を印加する。また、チャネルをオンさせ得るがメモリトランジスタMTa，MTbのしきい値電圧を変化させない程度に低く、かつ、それぞれ最適化された正の電圧を、制御ゲートCG1，CG2とワード線WLに印加する。このとき、読み出し対象の記憶部の蓄積電荷量、あるいは電荷の有無の違いによってチャネルの導電率が有効に変化し、その結果、記憶情報がドレイン側の電流量あるいは電位差に変換されて読み出される。もう一方のビットを読み出す場合は、そのビットが書き込まれた記憶部側がソースとなるように、ビット線電圧を切り替え、また制御ゲート電圧を切り替えることにより、上記と同様に読み出しを行う。

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【００３１】消去時には、チャネル形成領域ＣＨとソース・ドレイン領域Ｓ／Ｄ側が高く、制御ゲート電極ＣＧ１および／またはＣＧ２側が低くなるように、上記書き込み時とは逆方向の消去電圧を印加する。これにより、記憶部の一方または双方から蓄積電荷が基板ＳＵＢ側に引き抜かれ、メモリトランジスタが消去状態に戻る。なお、他の消去方法としては、ソース・ドレイン領域Ｓ／Ｄ側または基板内部の図示しないＰＮ接合付近で発生し蓄積電荷とは逆極性の高エネルギー電荷を、制御ゲートの電界により引き寄せることによって記憶部に注入する方法も採用可能である。

【００３２】つぎに、メモリセルの製造方法を、図５から図１１に示す断面図を参照しながら説明する。まず、基板ＳＵＢ上に、図１（Ａ）および図３に示すように、列方向に長い平行ストライプ状の誘電体分離層ＩＳＯを形成する。誘電体分離層ＩＳＯ上および誘電体分離層ＩＳＯ間の半導体活性領域上の全面に、図５に示すように、パッド層ＰＡＤ，酸化阻止層ＯＳおよび犠牲層ＳＦを順次形成する。酸化阻止層ＯＳは酸化されにくい緻密な膜であり、たとえば５０ｎｍ程度の窒化珪素の膜からなる。その下のパッド層ＰＡＤは、酸化阻止層ＯＳの基板ＳＵＢに対する密着性向上および応力緩和を目的として必要に応じて形成される薄い膜であり、たとえば５ｎｍ～８ｎｍ程度の二酸化珪素の膜からなる。犠牲層ＳＦは、酸化阻止層ＯＳに対してエッチング時の選択性が高い材料の膜、たとえば二酸化珪素膜からなり、その膜厚はビット線の高さに応じて決められる。

【００３３】この積層膜ＰＡＤ，ＯＳおよびＳＦを、レジスト等をマスクにパターンニングし、列方向に長い平行ストライプ状の開口部を形成する。この開口部内に、その長手方向に沿って誘電体分離層ＩＳＯと半導体活性領域とが交互に並んで露出する。

【００３４】Ｎ型不純物が高濃度にドープされた多結晶珪素を厚く堆積し、これを表面から研磨またはエッチバックすることにより、犠牲層ＳＦ表面で分離する。これにより、図７に示すように、積層膜ＰＡＤ，ＯＳおよびＳＦの開口部に埋め込まれたビット線ＢＬ１，ＢＬ２が形成される。ビット線ＢＬ１，ＢＬ２により、開口部内の底面に表出していた半導体活性領域が電気的に接続される。

【００３５】犠牲層ＳＦを選択的に除去した後、表出したビット線ＢＬ１，ＢＬ２の面を熱酸化して、たとえば数１０ｎｍ程度の誘電体膜ＤＦ１を形成する。誘電体膜ＤＦ１と酸化阻止層ＯＳの膜厚を最適化することにより、酸化阻止層ＯＳの端面側でも酸化が十分に進み、十分な厚さの誘電体膜ＤＦ１によりビット線ＢＬ１，ＢＬ２の表面を完全に覆うことができる。また、この加熱工程で、ビット線ＢＬ１，ＢＬ２を構成する多結晶珪素を固相拡散源としてＮ型不純物が半導体活性領域に拡散し、その結果、ソース・ドレイン領域Ｓ／Ｄが形成される。なお、この拡散のみではソース・ドレイン領域Ｓ／Ｄの深さおよび不純物濃度が不十分な場合は、追加の加熱をするか、あるいは、先の図６の工程で、開口部を通したイオン注入により必要な濃度の不純物を予め半導体活性領域に導入しておくとよい。

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【００３６】酸化阻止層ＯＳおよびパッド層ＰＡＤを順次除去し、表出したチャネル形成領域ＣＨと誘電体膜ＤＦ１の表面とを含む全面に、電荷蓄積膜ＣＳＦを形成する。なお、電荷蓄積膜ＣＳＦが図４に示す３層構造でボトム膜ＢＴＭを熱酸化により形成する場合は、ボトム膜ＢＭＴはチャネル形成領域ＣＨ表面にのみ形成される。

【００３７】不純物が十分にドープされた多結晶珪素を厚く堆積し、図３に例示し前述した制御パッドＣＰ１，ＣＰ２，ＣＰ３…を形成するためのエッチング保護層を多結晶珪素上の必要な箇所に形成した後、多結晶珪素をエッチバックする。これにより、ビット線ＢＬ１，ＢＬ２の両側面に対し、誘電体膜ＤＦ１，ＣＳＦを介在させた状態でサイドウォール形状の制御ゲートＣＧ１，ＣＧ２が形成される。また、同時に、制御ゲートＣＧ１，ＣＧ２，ＣＧ３，…に適宜接続された制御パッドＣＰ１，ＣＰ２，ＣＰ３…が形成される。このときの不純物が十分にドープされた多結晶珪素の厚さは、制御ゲート幅を決めるので厳密に制御される。その後、エッチング保護層を除去する。

【００３８】図１（Ｂ）の構造とするために、まず、制御ゲートＣＧ１，ＣＧ２をマスクとして電荷蓄積膜ＣＳＦをエッチングする。これにより、制御電極ＣＧ１，ＣＧ２間のチャネル形成領域ＣＨ上の電荷蓄積膜部分と、ビット線ＢＬ１，ＢＬ２の上方の電荷蓄積膜部分とが除去される。つぎに、熱酸化して、制御電極ＣＧ１，ＣＧ２表面と、制御ゲートＣＧ１，ＣＧ２間に露出したチャネル形成領域ＣＨの表面とに二酸化珪素膜を形成する。これにより、多結晶珪素または単結晶珪素の表面に単層の誘電体膜ＤＦ２が形成されるが、他の部分は誘電体膜であるため殆ど熱酸化されない。なお、ドープド多結晶珪素の熱酸化膜厚は、単結晶珪素の熱酸化膜厚の２倍ほどとなるので中央のＭＯＳトランジスタのゲート酸化膜厚が薄い場合でも配線間の絶縁性は十分確保される。続いて、全面にワード線ＷＬとなる導電材料を厚く堆積し、その上に行方向に長い平行ストライプ状のレジスト等のパターンを形成する。このパターンをマスクとしたＲＩＥ等の異方性が強いエッチングにより導電材料を加工して、ワード線ＷＬを形成する。また、図２（Ｂ）に示すワード線ＷＬのサイドウォールＷＬ’を形成する。以上により、メモリセルの基本構造が完成する。

【００３９】つぎに、本実施形態に係るメモリセル構造の、従来技術を示す前記論文に記載されたメモリセル構造に対する利点を説明する。なお、以下の説明では、上記論文に記載された断面構造において制御ゲートを２つのサイドウォールに分割した場合を比較例とするが、本

発明の利点は制御ゲートを分割しない場合でも同じである。図１２（Ａ）は、上記論文に記載されたセルの断面構造において、さらに制御ゲートを２つに分割した場合の行方向に沿った断面図である。図１２（Ｂ）は２メモリセルを中心に描いた平面図、図１３は制御パッドも含めたメモリセルアレイの平面図である。なお、これらの図において、本実施形態と共通する構成を指示する符号は、本実施形態で用いたものに統一している。

【００４０】この比較例のメモリセルは、ワードトランジスタＷＴと、これを挟んで２つのメモリトランジスタＭＴａ，ＭＴｂとが直列接続されている点を含む基本的なセル構成は本実施形態のメモリセルと共通している。

【００４１】ただし、比較例のメモリセルは、ワード線ＷＬに接続されるワードゲートＷＧを有し、その側面に電荷蓄積膜ＣＳＦを介在させた状態でサイドウォール状の制御ゲートＣＧ１，ＣＧ２，ＣＧ３を形成している点と、列方向のセル間分離を行う誘電体分離層ＩＳＯを有していない点で、本実施形態のメモリセルと構造上、大きく異なる。制御ゲートＣＧ１，ＣＧ２，ＣＧ３は列方向に長く形成する必要から、少なくとも、その形成時に補助層となるワードゲートＷＧも列方向に長い平行ストライプ状に形成する必要がある。しかし、その一方で、ワード線ＷＬ間を電気的に分離するためには、ストライプ状のワードゲートＷＧを各セルごとの孤立パターンに分断する必要がある。以上の点は、セル構造上明らかである。

【００４２】以下、比較例のセル構造から予想される製造方法を、順を追って簡潔に述べる。まず、単層の誘電体膜ＤＦとワードゲートＷＧとなる導電膜を基板ＳＵＢ上に積層させ、これらをパターンニングして列方向に長い平行ストライプ状のパターンを形成する。このパターン表面および基板ＳＵＢ表面を含む全面に、ＯＮＯ膜からなる電荷蓄積膜ＣＳＦを形成する。この状態で、ワードゲートＷＧとなる導電層間を埋め込むように不純物がドープされた多結晶珪素を厚く堆積し、たとえば図１３に示す制御パッドＣＰ１，ＣＰ２，ＣＰ３，…の位置など必要な箇所にエッチング保護層を形成し、その状態で、多結晶珪素を異方性の強い条件でエッチバックする。その結果、ワードゲートＷＧとなる導電層の両側面に電荷蓄積膜ＣＳＦを介在させた状態で多結晶珪素からなるサイドウォールが、制御ゲートＣＧ１，ＣＧ１，ＣＧ２，ＣＧ２，ＣＧ３，ＣＧ３，…として形成される。また、同時に制御パッドＣＰ１，ＣＰ２，ＣＰ３，…が形成される。多結晶珪素からなるサイドウォール（ポリサイドウォール）の表面を熱酸化法により酸化した後、ポリサイドウォールおよびワードゲートＷＧとなる導電層をマスクとし、かつポリサイドウォール間の電荷蓄積膜ＣＳＦをスルー膜としたイオン注入により、ポリサイドウォール間の基板表面領域にＮ型不純物を導入しソース・ドレイン領域Ｓ／Ｄを形成する。その後、ポリサイドウォール間のスペースを二酸化珪素などの誘電体で埋め込んだ後、研磨またはエッチバックにより、その表面高さがほぼワードゲートＷＧとなる導電層の高さと等しくなるように誘電体の表面を平坦化する。この平坦化は、ワードゲートＷＧとなる導電層表面が露出するが、ポリサイドウォール表面は熱酸化膜の存在により露出しない程度で止める。続いて、平坦化面上にワード線ＷＬとなる導電物質を堆積し、その上に行方向に長い平行ストライプ状のレジストを形成する。レジストをマスクとして導電体をエッチングしワード線ＷＬ間を分離する。また、連続してワード線ＷＬ間の下地に露出した導電層をエッチングにより分断する。これにより、ワードゲートＷＧがセルごとに孤立したパターンにて形成される。

【００４３】この比較例の第１の問題は、最終工程で、ワードゲートＷＧとなる導電層をセルごとのパターンに分断する際に多結晶珪素の残渣が生じやすいことである。すなわち、前記したようにワードゲートＷＧとなる導電層の断面が台形状であることに起因して、これを分断する際には逆テーパ状の側面を有した穴を掘ることとなり、その結果、表面の開口部から見て影となる部分の最も奥まった箇所、すなわち図１２（Ｂ）に示すように側面の下辺に沿った部分に筋状に多結晶珪素が残りやすい。このような多結晶珪素の残渣は、ワードゲートＷＧ間を電気的にショートさせるため、このメモリセルアレイはワード線ショート不良となる。

【００４４】本実施形態に係るセル構造においては、ワードゲートＷＧとなる導電層を有していないため、これを分断する必要がない。また、ワード線ＷＬを分離する際にエッチング除去する箇所の下地にはサイドウォール形の制御ゲート形状を反映して順テーパの側面を有している。したがって、この部分に導電物質が残り難いという利点がある。

【００４５】比較例の第２の問題点は、本実施形態のように誘電体分離層ＩＳＯを有していないため、書き換え動作を何度も繰り返すうちに記憶部に隣接した電荷蓄積膜ＣＳＦの領域に電荷が定常的に溜まりやすくなることである。とくに書き換え動作で注入だけが行われる電荷、たとえば消去のために注入される逆極性の電荷（正孔）は、注入だけされて意図的に引き抜かれることがないため、この領域に徐々に留まりやすい。その結果、チャネルの外側にリークパスができやすくなる。図１２（Ｂ）は、この電荷の残留領域とリークパスの方向を示す。

【００４６】本実施形態では、図２（Ａ）においてチャネル形成領域ＣＨに接した電荷蓄積膜ＣＳＦの部分が記憶部となるが、その記憶部の隣接領域は誘電体分離層ＩＳＯ上に乗り上げている。したがって、この隣接領域に電荷が定常的に溜まることがあっても、その電荷によってチャネルが影響を受けず、リークパスが生じないという利点がある。なお、誘電体分離層をＬＯＣＯＳ法やＳ

ＴＩ法により形成した場合は、基板表面領域が絶縁化されるため更にリーク電流が発生しにくい。

【００４７】比較例の第３の問題点として、図１３に示すように、制御ゲートがワードゲートＷＧとなる導電層の周囲を一周したに環状に形成されるため、この制御ゲートを、たとえば導電層の短辺側で２か所切断する必要がある。なぜなら、１メモリセル内の２つの制御ゲートＣＧ１とＣＧ２，ＣＧ２とＣＧ３，…は、独立に異なる電圧を印加できないと効率良く２ビット記憶動作させることが困難だからである。

【００４８】本実施形態のセル構造では、１メモリセル内の２つの制御ゲートＣＧ１とＣＧ２，ＣＧ２とＣＧ３，…は、図３に示すように、形成時点で既に分離されている。したがって、本実施形態では、隣接する制御ゲートＣＧ１とＣＧ１，ＣＧ２とＣＧ２，…を同電位で用いる限りは制御ゲートを切断するための工程は不要であるという利点がある。なお、ＶＧセルアレイのシリアルアクセス動作の自由度を高めるために制御ゲートの全てを独立に制御させたい場合は、図３において制御ゲートＣＧ１とＣＧ１，ＣＧ２とＣＧ２，…をそれぞれ切断する必要が生じ、制御ゲートの切断箇所が比較例と異なるだけで、切断する箇所の数は同じとなる。

【００４９】その他、本実施形態では、補助層が導電物質（たとえば不純物をドープした多結晶珪素）からなり、ビット線を半導体内に埋め込まれた不純物領域のみで形成した比較例と比べビット線ＢＬ１，ＢＬ２，…の抵抗が低減されている。また、本実施形態では、ワードトランジスタＷＴのチャネル長を最小線幅Ｆより小さくすることができる。ワードトランジスタＷＴのソースとドレインはメモリトランジスタＭＴａ，ＭＴｂのチャネルであることから、ワードトランジスタＷＴのチャネル長を微細化してもパンチスルーが問題となり難い。

【００５０】本実施形態では、本発明の技術的思想の範囲内で種々の改変が可能である。たとえば、制御ゲートを形成する対象となる補助層は、多結晶珪素に限らず非晶質珪素、その他の導電体から構成することもでき、また誘電体から構成することも可能である。その場合、誘電体分離層ＩＳＯの下にソース・ドレイン領域を埋め込んで形成するか、誘電体分離層ＩＳＯを記憶部の両側までとしソース・ドレイン領域Ｓ／Ｄ上で切断する必要がある。その結果、ソース・ドレイン領域Ｓ／Ｄが列方向に長いライン状に形成され、このソース・ドレイン領域Ｓ／Ｄをビット線として用いる。

【００５１】また、図８の工程において多結晶珪素の表面に熱酸化による誘電体膜ＤＦ１を形成せずに、図９の工程の電荷蓄積膜ＳＣＦの形成を行ってもよい。その場合、図１１の工程において、電荷蓄積膜ＳＣＦのエッチングによりビット線ＢＬ１，ＢＬ２，…となる多結晶珪素の上面が露出するが、その後、制御ゲートＣＧ１，ＣＧ２，…の表面を熱酸化する際に、このビット線となる多結晶珪素の上面にも熱酸化され二酸化珪素膜が形成されることから、ワード線との絶縁分離膜は十分になされる。この方法では、図５におけるパッド層ＰＡＤおよび酸化阻止層ＯＳの成膜工程と、その後の除去工程、および図８における熱酸化工程が不要であり、その分、工程が簡略化される利点がある。

【００５２】さらに、制御ゲートＣＧ１，ＣＧ２，…の形状は、導電体または誘電体からなる補助層（上記説明では、ビット線ＢＬ１，ＢＬ２，…）の側面に形成されたサイドウォール形状に限定されない。たとえば、図１４に示すように、制御ゲートＣＧ１，ＣＧ２，…を、ビット線ＢＬ１，ＢＬ２，…の側面および上面を覆う形状としてもよい。ただし、この形状は、ビット線を挟んで異なるセルに属する制御ゲートを電気的に同電位で用いる用途に限定される。また、この構成では、必然的に、電荷蓄積膜ＣＳＦも、ビット線ＢＬ１，ＢＬ２，…の側面および上面を覆う形状となっている。先に説明した図１１の電荷蓄積膜ＣＳＦの分離工程において、ビット線上の電荷蓄積膜部分は、制御ゲートＣＧ１，ＣＧ２，…により保護されるからである。

【００５３】以下、この制御ゲートＣＧ１，ＣＧ２，…の形成方法を２例、図面を参照しながら説明する。第１の方法を、図１５～図１７に示す。この製造方法は、先に説明し図１０に示すサイドウォール形の制御ゲートの形成工程を、図１５と図１６に示す工程で置き換えることで実施できる。

【００５４】図５～図９と同じ工程を経て、ビット線ＢＬ１，ＢＬ２、ソース・ドレイン領域Ｓ／Ｄ、誘電体ＤＦ１および電荷蓄積膜ＣＳＦの形成を行った後、図１５に示すように、全面に、たとえば多結晶珪素または非晶質珪素などからなる導電膜ＣＧＦを形成する。また、ビット線ＢＬ１，ＢＬ２上に位置する導電膜ＣＧＦ部分の上に、フォトリソグラフィによりレジストパターンＲ１を形成する。

【００５５】このレジストパターンＲ１をマスクとしたエッチングにより、導電膜ＣＧＦをパターンニングする。これにより、図１６に示すように、チャネル形成領域の中央部の上方で分離した制御ゲートＣＧ１，ＣＧ２が形成される。このときのエッチングは、異方性が適度に強く、レジストパターンＲ１がやや後退する条件が望ましい。エッチング中にレジストパターンＲ１が膜減りすることにともなって、レジストパターンＲ１のエッジが後退し、その結果、制御ゲートＣＧ１，ＣＧ２の側面の主な領域が順テーパとなるからである。なお、エッジの後退を容易化するために、たとえば比較的高温のポストベークなどによって、レジストパターンＲ１のエッジを予めラウンドさせておいてもよい。

【００５６】図１７に示すように、この制御ゲートＣＧ１，ＣＧ２をマスクとしたエッチングを行い、電荷蓄積膜ＣＳＦを分離する。また、図１４の構造とするため

に、前記したと同様な方法によって、誘電体膜ＤＦ２およびワード線ＷＬを形成し、当該メモリセルの基本構造を完成させる。

【００５７】第２の方法は、導電膜ＣＧＦの加工時のマスク層を下地形状に対し自己整合的に形成する方法である。第２の方法を、図１８～図２２に示す。この製造方法は、先に説明し図１０に示すサイドウォール形の制御ゲートの形成工程を、図１８～図２２に示す工程で置き換えることで実施できる。

【００５８】図５～図９と同じ工程を経て、ビット線ＢＬ１，ＢＬ２、ソース・ドレイン領域Ｓ／Ｄ、誘電体ＤＦ１および電荷蓄積膜ＣＳＦの形成を行った後、図１８に示すように、全面に、たとえば多結晶珪素または非晶質珪素などからなる導電膜ＣＧＦを形成する。続いて、たとえば窒化珪素などからなる酸化阻止膜ＯＳＦを導電膜ＣＧＦ表面に薄く形成する。また、レジストを塗布しベーキング後にエッチバックして、表面の凹部をレジストＲ２により埋め込む。

【００５９】この状態でレジストＲ２をマスクとしたエッチングにより、図１９に示すように、ビット線ＢＬ１，ＢＬ２の上方に位置する酸化阻止膜ＯＳＦの一部を除去する。

【００６０】レジストＲ２を除去後、酸化阻止膜ＯＳＦの周囲に露出した導電膜ＣＧＦを選択的に熱酸化して、図２０に示すように、ビット線ＢＬ１，ＢＬ２の上方に誘電体膜ＤＦ２を形成する。図２１に示すように、酸化阻止膜ＯＳＦを除去する。

【００６１】誘電体膜ＤＦ２をマスクとしたエッチングにより、導電膜ＣＧＦをパターンニングする。これにより、図２２に示すように、チャネル形成領域の中央部の上方で分離した制御ゲートＣＧ１，ＣＧ２が形成される。このときのエッチングは、異方性が適度に強く、誘電体膜ＤＦ２がやや後退する条件が望ましい。誘電体膜ＤＦ２は、酸化阻止膜ＯＳＦをマスクとした選択酸化により形成することから、いわゆるＬＯＣＯＳのバーズビークと同様に、そのエッジ部分において先端ほど膜厚が薄くなっている。したがって、制御ゲートのエッチング中に誘電体膜ＤＦ２が膜減りすると、それにともなって誘電体膜ＤＦ２のエッジが後退し、その結果、制御ゲートＣＧ１，ＣＧ２の側面の主な領域が順テーパとなる。

【００６２】その後、この制御ゲートＣＧ１，ＣＧ２をマスクとしたエッチングを行い、電荷蓄積膜ＣＨＳを分離する。また、図１４の構造とするために、前記したと同様な方法によって、制御ゲートＣＧ１，ＣＧ２の側面に誘電体膜ＤＦ２を形成し、ワード線ＷＬを形成し、当該メモリセルの基本構造を完成させる。

【００６３】

【発明の効果】本発明に係る不揮発性半導体記憶装置およびその製造方法によれば、従来例のようにワードゲート電極とワード線を接続する工程が不要であり、また第２制御電極を加工する際に、第２制御電極間をショートするような導電物質の残渣が発生しない。第１制御電極に沿った方向で記憶部より外側の近接領域に制御できない電荷が定常的に溜まる場合でも、誘電体分離層の存在により、その電荷のチャネルへの影響が格段に弱められ、その結果、書き換え動作を繰り返してもリーク特性が劣化しない。１メモリセル内の２つの第１制御電極を形成する時点で既に両者が分離されており、これを独立に制御するために分離する工程が不要である。補助層が導電物質からなる場合、ビット線を半導体内に埋め込まれた不純物領域のみで構成した場合に比べビット線の抵抗が格段に低減された。また、第１制御電極を補助層の側面と上面を覆う形状とした場合、第１制御電極の抵抗がサイドウォール形に比べ低減された。さらに、第２制御電極のラインとスペースの幅をリソグラフィの最小限界値で形成しても、第２制御電極の合わせずれによりリーク電流が増大したりチャネル幅が減少することがなく、その結果、読み出し信号のＳ／Ｎ比が低下しない。

【図面の簡単な説明】

【図１】（Ａ）は実施形態に係るメモリセルの平面図である。（Ｂ）は（Ａ）のＡ－Ａ線に沿った断面図である。

【図２】（Ａ）は実施形態に係るメモリセルにおいて、図１（Ａ）のＢ－Ｂ線に沿った断面図である。（Ｂ）は図１（Ａ）のＣ－Ｃ線に沿った断面図である。

【図３】実施形態に係る不揮発性メモリにおいて、制御ゲートの電極引き出し用のパッドを含めて示すメモリセルアレイの平面図である。

【図４】実施形態に係る図１（Ａ）のメモリセルの主要部分を拡大して示す断面図である。

【図５】実施形態に係るメモリセルの製造において、犠牲層の成膜後の断面図である。

【図６】実施形態に係るメモリセルの製造において、犠牲層等にビット線のパターンを開口した後の断面図である。

【図７】実施形態に係るメモリセルの製造において、ビット線形成後の断面図である。

【図８】実施形態に係るメモリセルの製造において、ビット線の表面を熱酸化した後の断面図である。

【図９】実施形態に係るメモリセルの製造において、電荷蓄積膜を形成した後の断面図である。

【図１０】実施形態に係るメモリセルの製造において、制御ゲート形成後の断面図である。

【図１１】実施形態に係るメモリセルの製造において、制御ゲートをマスクとした電荷蓄積膜の一部を除去後の断面図である。

【図１２】（Ａ）は実施形態の比較例に係るメモリセルの構造を示す概略断面図である。（Ｂ）は実施形態の比較例に係る２つのメモリセルを中心としたメモリセルアレイの平面図である。

【図１３】実施形態の比較例に係るメモリセルアレイと制御パッドの平面図である。

【図１４】実施形態の制御ゲート形状の変形例を示す、図１（Ａ）のＡ－Ａ線に沿った断面図である。

【図１５】変形例の制御ゲートを形成する第１の方法に関し、レジストパターンの形成後の断面図である。

【図１６】変形例の制御ゲートを形成する第１の方法に関し、制御ゲートのエッチング後の断面図である。

【図１７】変形例の制御ゲートを形成する第１の方法に関し、電荷蓄積膜のエッチング後の断面図である。

【図１８】変形例の制御ゲートを形成する第２の方法に関し、レジストの埋込後の断面図である。

【図１９】変形例の制御ゲートを形成する第２の方法に関し、酸化阻止膜の一部除去後の断面図である。

【図２０】変形例の制御ゲートを形成する第２の方法に関し、誘電体膜の形成後の断面図である。

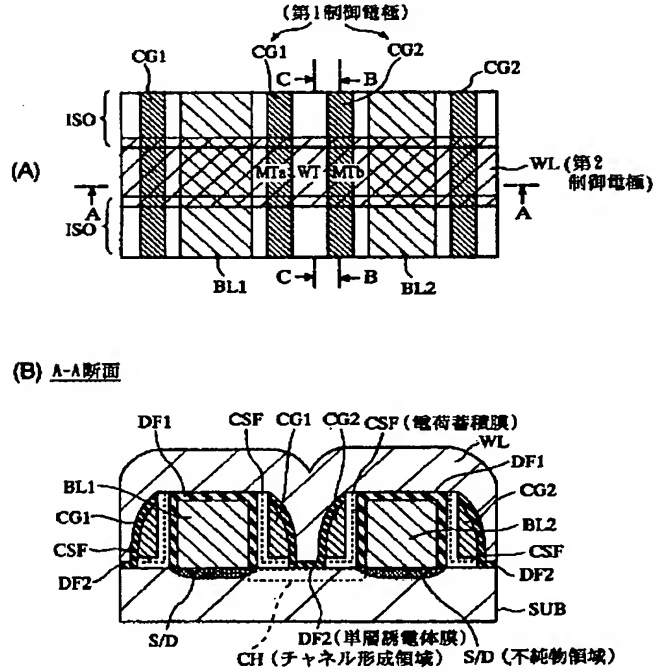
【図２１】変形例の制御ゲートを形成する第２の方法に関し、残りの酸化阻止膜の除去後の断面図である。

【図２２】変形例の制御ゲートを形成する第２の方法に関し、制御ゲートのエッチング後の断面図である。

【符号の説明】

ＭＴａ，ＭＴｂ…メモリトランジスタ、ＷＴ…ワードトランジスタ、ＷＬ，ＷＬ１，ＷＬ２，ＷＬ３…ワード線（第２制御電極）、ＷＬ’…サイドウォール、ＢＬ１，ＢＬ２，ＢＬ３…ビット線、ＣＧ１，ＣＧ２１，ＣＧ３…制御ゲート（第１制御電極）、ＩＳＯ…誘電体分離層、ＳＵＢ…基板（半導体）、Ｓ／Ｄ…ソース・ドレイン領域（不純物領域）、ＣＨ…チャネル形成領域、ＤＦ１…誘電体膜、ＤＦ２…単層の誘電体膜、ＣＳＦ…電荷蓄積膜、ＣＰ１，ＣＰ２，ＣＰ３…制御パッド（第１制御電極の引き出し領域）、ＢＴＭ…ボトム膜、ＣＳ…中間の電荷蓄積膜、ＴＯＰ…トップ膜、ＰＡＤ…パッド層、ＯＳ…酸化阻止層、ＳＦ…犠牲層、ＷＧ…ワードゲート、ＯＳＦ…酸化阻止膜、Ｒ１，Ｒ２…レジスト。

【図１】



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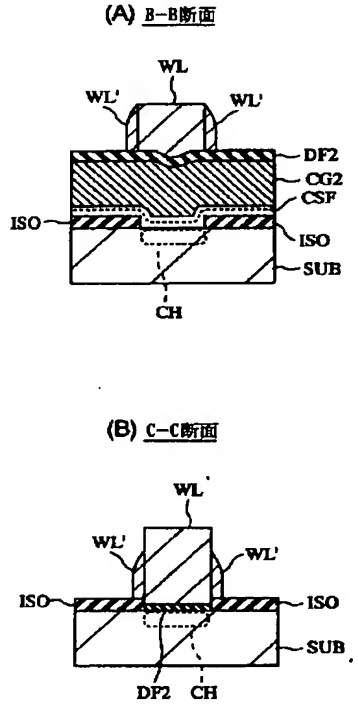

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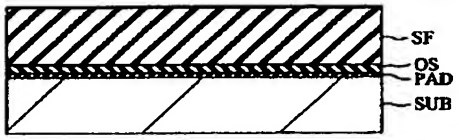

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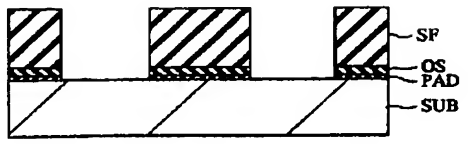

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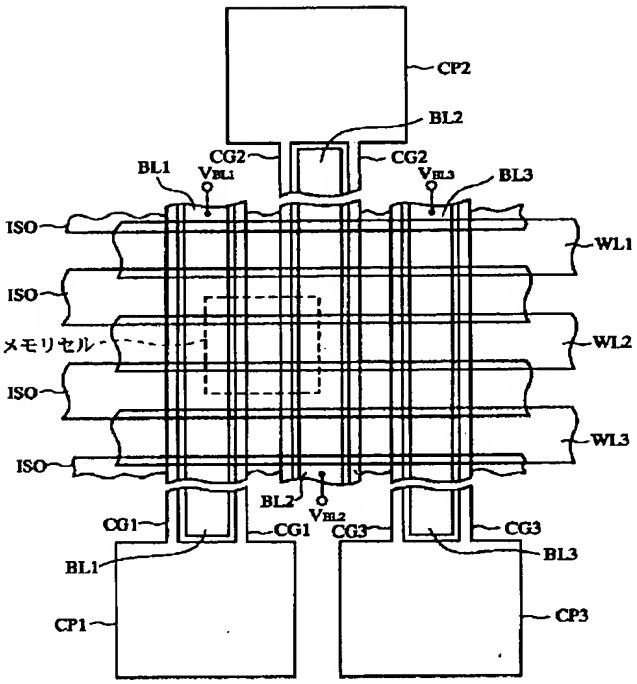

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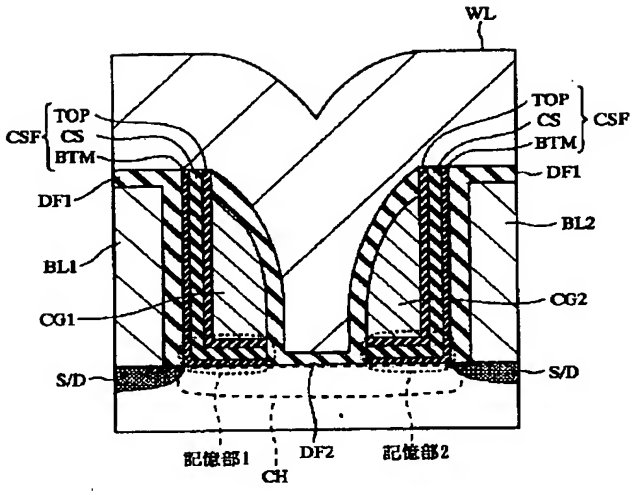

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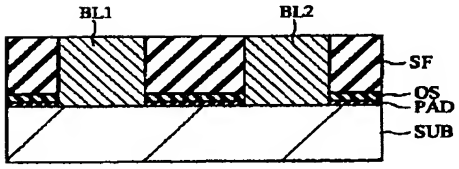

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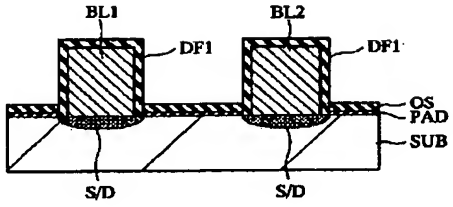

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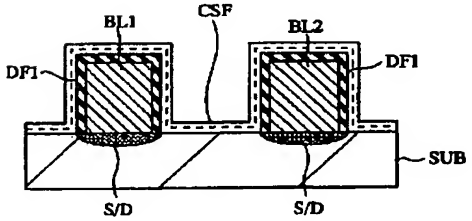

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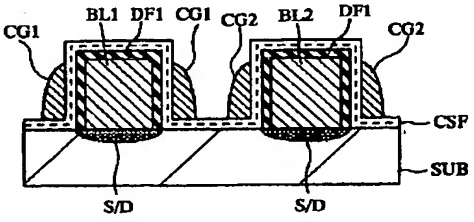

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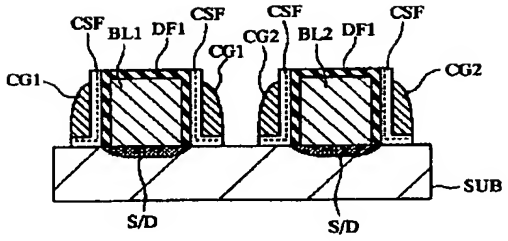

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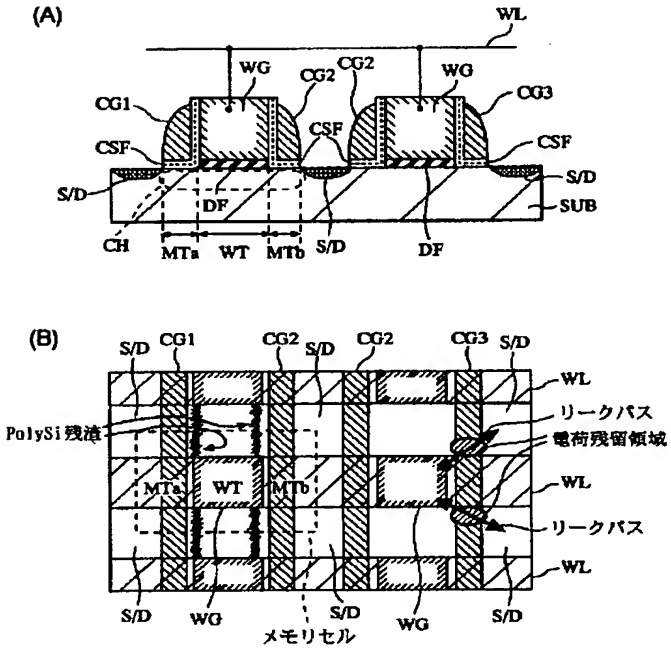

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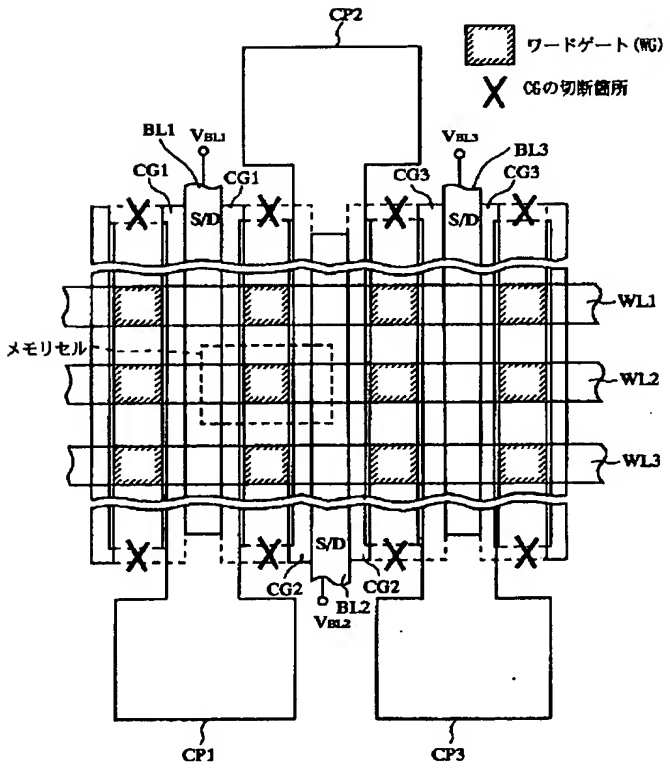

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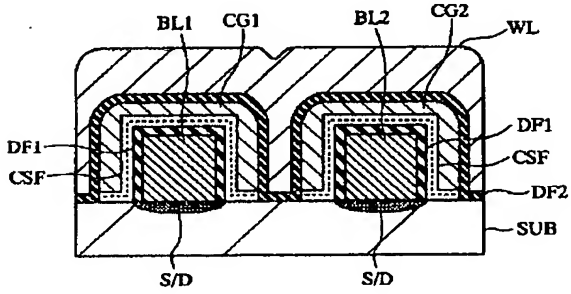

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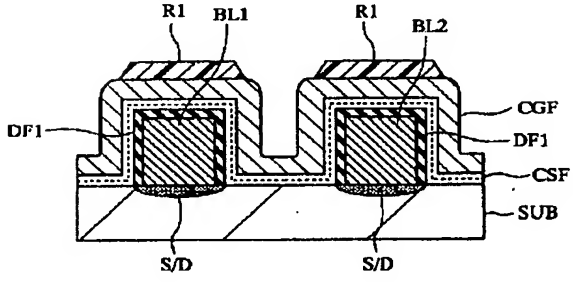

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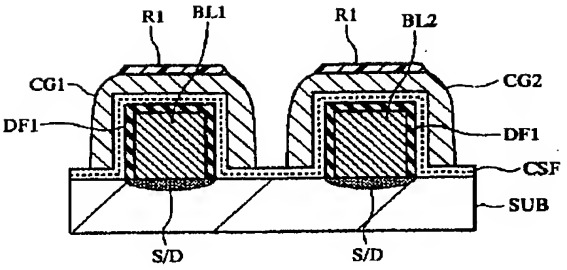

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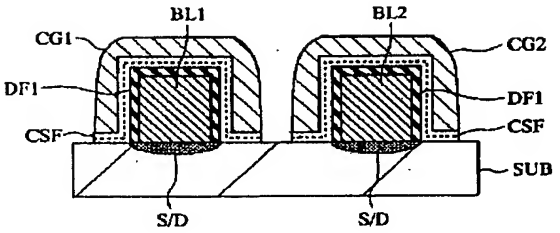

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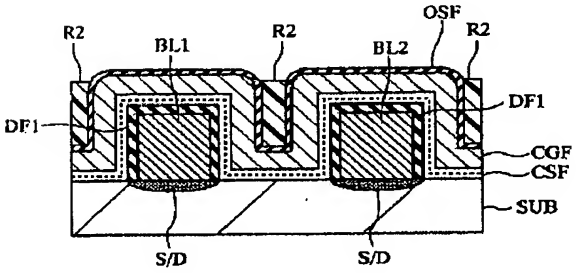

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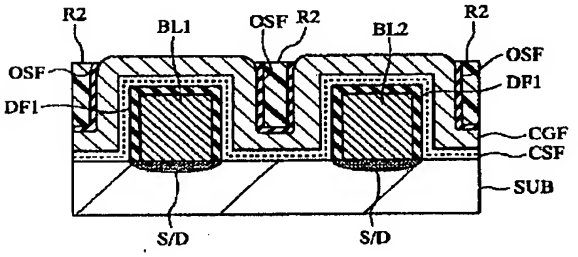

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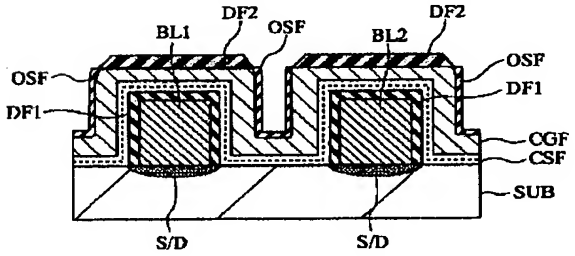

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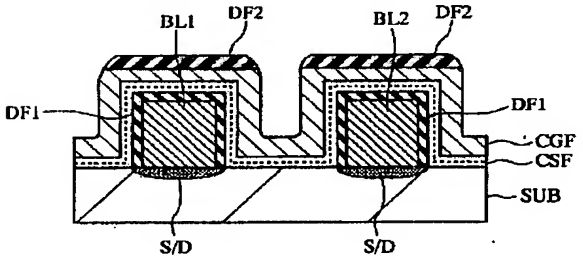

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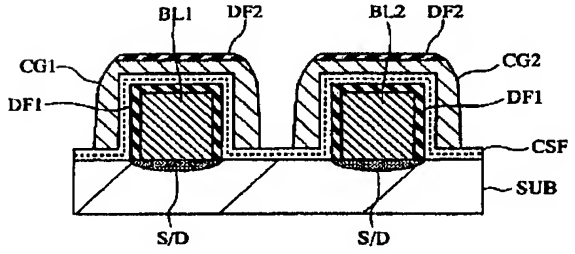

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